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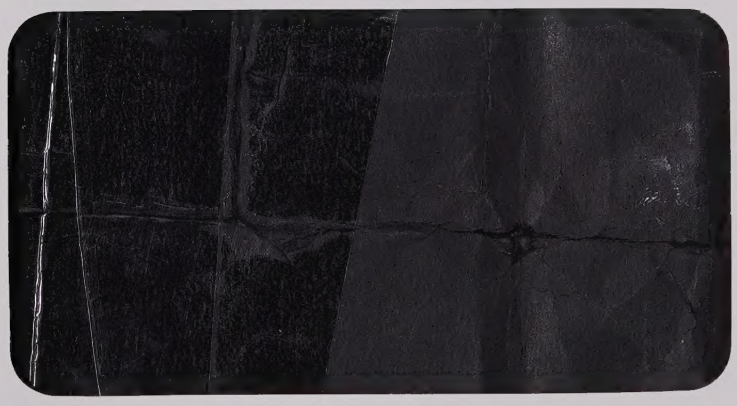
GOULD



DIGITAL STORAGE OSCILLOSCOPE 1425

Instruction Manual

GOULD

Hainault Essex England

Telephone 01-500 1000
Telegrams Attenuate Ilford
Telex 263785

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Introduction

Section 1

The Gould 1425 provides a combination of digital storage and real time facilities, and caters for measurements from D.C. to 20MHz with a flicker free display of a full cycle down to 0.002Hz. The digital method of storage provides many advantages notably the facilities for pretrigger viewing and the ability to store a waveform indefinitely and compare waveforms.

It features two identical input channels with a maximum sensitivity of 2mV/div and a bandwidth from DC> up to 20MHz. The channels may be displayed separately or together in both STORE and the conventional NORMAL modes. The ability to display the sum or difference of the channels and an X-Y mode operation are available in NORMAL mode. The timebase ranges from 0.5 microsecs/div to 0.2sec/div in NORMAL mode with additional ranges down to 50s/div in STORE mode. A x 10 facility expands the upper limit to 50ns/div. In NORMAL and certain of the STORE modes independent variable sweep rate and separate controls are provided.

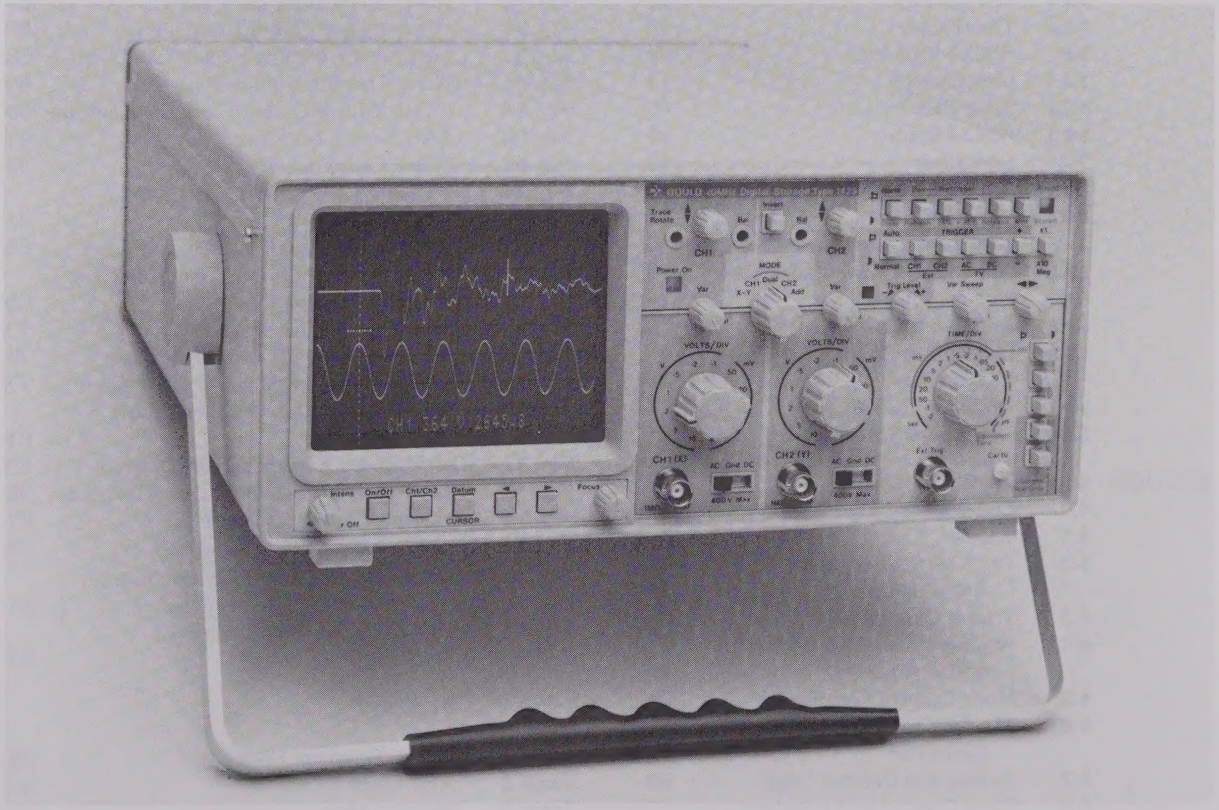
A pair of cursors are available on either trace for convenience in making measurements on the traces. A 16 character display on the screen shows the time and voltage differences between the two cursors.

In addition the 1425 has an RS423 serial interface which enables the instrument to send stored data to an external controller and if required receive new data for display. The interface will also allow certain digital functions to be remotely programmed.

The trigger facilities available are comprehensive with D.C. and A.C. coupling available and an auto free run facility to enable true location in the absence of a trigger. An active TV sync. separator is provided for viewing video waveforms.

Many additional features are provided with the 1425 such as the option of an analogue or digital plot which is fitted as standard as well as a 1KHz calibrator, a D.C. coupled Z modulation input, a trace rotation control, a line trigger output and an optional waveform processing unit.

The instrument is readily portable and the use of an uncommited logic array has reduced both the number of components and board area. This has additional benefits in terms of reliability, power consumption and ease of maintenance.



DISPLAY

CRT 8 x 10cm rectangular mono-accelerator.

EHT 2kV (Trace rotation by front panel preset).

VERTICAL DEFLECTION

Two identical input channels CH1 and CH2.

Bandwidth –3db
d.c. to 20MHz (2Hz to 20MHz on a.c.)

Sensitivity 2mv/div to 10V/div in 1–2–5 sequence.

Accuracy ±3%.

Variable Sensitivity >2.5:1 range allows continuous adjustment of sensitivity 2mV/div to 25V/div.

Input Impedance: 1MΩ/28pF.

Input Coupling: DC–GND–AC.

Input Protection 400V d.c. or pk a.c.

HORIZONTAL DEFLECTION

Normal Mode Sweep Rate 0.5μs/div to 0.2sec/div, 18 ranges in 1–2–5 sequence.

Accuracy ±3% (to 200ns/div).

Variable Sweep >2.5:1 allows continuous coverage from 0.5μs/div to 0.5sec/div.

Store Modes Sweep Rate 0.5μs/div to 50sec/div, 25 ranges in 1–2–5 sequence.

Accuracy ±3% (to 200ns/div).

Variable Sweep >2.5:1 allows continuous coverage from 0.5μs/div to 50μs/div (sampling only).

X Expansion X10 push button gives fastest speed of 50ns/div. Accuracy ±3% (50ns ±5%).

TRIGGER

Variable level control with Auto trigger facility. In Auto, the timebase free-runs when insufficient signal (20Hz to 20MHz) is present or when the selected level is outside the range of the input signal.

Source Internal CH1 or CH2, External.

Slope Positive or negative.

Coupling DC, AC or TV (active sync separator with line/frame selected by timebase switch between 50 and 100μs/div).

Sensitivity Internal: DC coupled 0.3div to 2MHz, 1 div to 20MHz.
AC coupled 0.3div 10Hz–2MHz.
1 div, 4Hz–20MHz.
External: DC coupled 150mV to 2MHz, 600mV to 20MHz.
AC coupled 150mV, 10Hz to 2MHz.
600mV, 4Hz to 20MHz.

External Input Impedance 100kΩ/10pF.

External Input Protection 250V d.c. or pk a.c.

DISPLAY MODES

Single trace CH1 or CH2.

Dual trace In Normal, Chopped or Alternate Modes automatically selected by the timebase switch. Between 0.5μs/div and 0.2ms/div the Alternate Mode is selected whilst on ranges slower than 0.2ms/div Chop Mode is selected. The chop frequency is 500kHz.
(In store modes simultaneous capture).

Add CH1 and CH2 added to give the algebraic sum of the two channel inputs (Normal mode only).

Invert CH2 CH2 may be inverted. When used in conjunction with Add mode it gives the algebraic difference of the two channels.

X–Y CH1 input gives X deflection and CH2 input gives Y deflection. (Normal mode only).

DIGITAL FACILITIES

Store Size 1024 x 8-bits per channel.

Vertical Resolution 1 in 256 approx. 28.5 steps/div.

Horizontal Resolution 1 in 1024 approx. 100 samples/div. (0.05ms/div range on Dual is 50 samples/div).

Expansion x10 reduces the horizontal resolution by ten on all ranges.

Sample Rate: 2MHz (0.5μs) reducing in proportion with timebase.

Dot Joining Linear interpolation between samples.

DISPLAY MODES

Roll Stored data and display updated continually. (timebase ranges 50sec/div to 0.05ms/div).

Refreshed Stored data and display updated by triggered sweep. (timebase ranges 50sec/div to 0.05ms/div).

Equivalent Sample Time This mode is automatically selected when timebase ranges of 20μs/div to 0.5μs/div are used. It enables repetitive waveforms up to 20MHz to be stored with full horizontal resolution.

Single Shot Freezes store at end of triggered sweep.

Hold–All Freezes store immediately.

Hold–CH2 Freezes CH2 data immediately.

Pretrigger Storage Available in Roll mode only, switchable for 0%, 25%, 75% and 100% of full store pre-trigger.

CURSOR MEASUREMENTS

Controls On/Off control of Alpha-numerics and cursors. Selection of channel for measurement CH1/CH2. Set datum to current cursor position.
◄ ► Dual speed cursor position (left/right) to enable time and voltage difference measurement.

Accuracy Time ±0.1% of full scale deflection on ranges 50secs/div – 0.05ms/div, ±3% of full scale deflection on ranges 20μs/div – 0.5μs/div. Voltage 3% of reading ±0.5% of full scale ±1 digit.

INPUT/OUTPUT FACILITIES

ANALOGUE PLOT OUTPUT

Analogue output of the stored display.

Y Output Channel 1 or Channel 2 selected by Plot 1 or Plot 2 push switch for the respective channel via 4mm socket. Amplitude 100mV/div (nominal).

X Output X ramp via 4mm socket. Amplitude 100mV/div (nominal).

Output Sweep Rate Selected by Time/cm (main time-base range 50sec/div to 50ms/div in 1–2–5 sequence.

Output Impedance 100Ω.

Pen Lift Output High output to indicate penlift. TTL open collector. Maximum Voltage 15V. Maximum Sink Current 8mA.

DIGITAL PLOT

Output of data and range via RS423 interface to a digital plotter.

Scale Automatically printed.

Graticule Available for plotting at the completion of a plot cycle by selection of 'set datum'.

Colours Colour pens automatically selected for CH1, CH2 and graticule when available on plotter.

RS423 INTERFACE

Read and Write Functions
Baud rate
Stored Data input/output
Data Format: Binary, Decimal, Hexadecimal, Octal and string length.
Timebase range (limited write)
Hold display and Hold CH2
Digital plot

Write Only
Arm and Release
Plot
Local
Text

Read Only
CH1, CH2 and Dual
Attenuator and Timebase setting current and stored

Additional Facilities
Line output 1V approx.

Calibrator 1V ±2% square wave at approx. 1kHz.

Z Mod Input DC coupled, 2V visible mod.
Sensitivity +15V cut off sensitivity.
Input impedance 10kΩ/10pF approx.
Maximum input 100V d.c. or pk a.c.

Supply 100V, 120V, 220V and 240V ±10%.
45 to 400Hz, 40VA approx.

Safety Designed for IEC 348 Cat 1.

Operating Temperature Range 0 to 50°C (+15°C to 35°C for full accuracy).

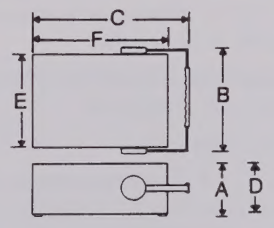
Humidity IEC 68-2Ca Operating 45°C at 95% RH
IEC 68-2Db Cycling non-operating 25°C to 45°C 95% RH, 6 cycles, 144 hours.

Dimensions Overall (mm, inches in bracket):

A	B	C
140	335	510
(5.5)	(13.2)	(20.0)

Excluding handle and feet:

D	E	F
134	305	460
(5.2)	(12.0)	(18.1)



Weight 7.5kg approx. (16lb 9oz)

Accessories Supplied Handbook PN 453639
Mains Lead PN 402001

Optional Accessories

Probe Kit PB12
A passive probe kit with switched X1 and X10 attenuators.
X10 attenuation input impedance is 10MΩ/11.5 pF.

Probe Kit PB13
A X10 passive probe with 1.5m of cable. Input impedance 10MΩ/11.5pF.

Probe Kit PB17
A X100 passive probe with 1.5m of cable.
Input impedance 100MΩ/4.5pF.
Working voltage 1.5kV inc pk a.c.

Viewing Hood PN450401

Front Panel Cover PN453709

Rack Mount Kit PN453710

Rack Mount Kit with slides PN453711

Trolley Type TR7 General Purpose

Protective Carrying Case PN453712 – A strong case which completely encloses the oscilloscope with 3 thicknesses of padded material covering the front panel.

Waveform Processor Type 125
Available in the form of an upgrade kit (if not bought with 1425), it allows the following extra functions selected by means of a keypad, connected by a cable to the rear of the 1425.

SIGNAL CAPTURE FUNCTIONS

Signal Averaging Up to 256 averages allowing 1, 4, 8, 16, 32, 64, 128, 256 averages.

Capture Arm the scope for a signal capture.

Capture & Repeat Arm the scope for a signal capture and automatically apply the previously used post storage functions.

POST-STORAGE FUNCTIONS

CH1 x CH2: Displays (CH1 x CH2)/5.01

CH1 + CH2: Displays the addition of the two signals.

CH2 – CH1: Displays the difference between the two signals.

CH1 – CH2: Displays the difference between the two signals.

(datum referred to centre line of screen)

Copy CH1 – CH2 Copies store 1 to store 2 or
CH2 – CH1 store 2 to store 1.

Trace Magnification/Attenuation Multiple trace from x3.98 to x0.06 in 250 steps selectable by step control. Gain is displayed on the screen.

Filter 6 selectable stages of filtering per timebase range.

$$\text{Cut-off frequency} = \frac{8.14}{Tx2^{n-1}} \quad \text{Hz}$$

Where: T = Timebase range in s/cm and
n = filter stage from 1 to 6.

Invert Invert trace about the centre line.

Restore Displays trace as if the last post-storage function selected was removed.

Position Moves trace and datum in X and Y planes and cursor in X plane.

Frequency Calculate and display signal frequency as measured between two cursors.

BACK-UP STORES

Store Number Choose 1 of 5 stores to retrieve or save.

Save/Recall Save or recall selected store.

INTERNATIONAL SAFETY WARNING
(as required for I.E.C. 348 Class I)

This instruction manual contains information and warnings which must be observed by the user to ensure safe operation and retain the apparatus in a safe condition. The instrument has been designed for indoor use within the specified limits of temperature. It should not be switched on if there are obvious signs of mechanical damage and it should not be used under wet conditions.

EARTHING
The instrument must be operated with a protective earth connected via the appropriate (yellow/green) conductor of the supply cable. This is connected to the instrument before the line and neutral supply connections when the supply socket is inserted into the plug on the back of the instrument. If the final connection between the instrument and the supply is made elsewhere, the user must ensure earth connection is made before line and neutral.

If any supply cable other than that supplied with the instrument is used, it must carry an adequate protective earth conductor.

Any interruption of the protective earth conductor inside or outside the instrument is likely to make the instrument dangerous. Intentional interruption is prohibited.

Signal connections into the instrument should be connected after and disconnected before the protective earth connection is made, i.e. the supply lead must be connected at all times that signal leads are connected.

LIVE PARTS
The instrument is safe to operate with the covers fitted and these must not be removed under normal usage. The covers protect the user from live parts and they should be removed only by suitably qualified personnel for maintenance or repair purposes. (see maintenance section).

VENTILATION
The 1425 relies on convection cooling and must not be operated in a position which restricts the external circulation of air.

3.1 CONNECTION TO THE SUPPLY

1. Before connecting the 1425 to the supply, check that the supply range switches are set to suit the supply voltage to be used and that the correct fuse is fitted. Note that the fuse has to be changed when switching between the 100V and 220V ranges. The switches and fuse holder are mounted on the back panel of the instrument. Do not operate the range selection switches while the 1425 is switched on.

3.2 OBTAINING A TRACE

1. After connection to the supply, switch on by turning the INTENSITY control clockwise away from the OFF position. Check that the POWER indicator l.e.d. lights.

2. Set the:
   Set NORM/STORE switch to NORM.
   MODE switch to CH1.
   CH1 Y shift control (vert. arrows) to approx. mid setting.
   CH1 VAR SENS control fully clockwise to the CAL position.
   CH1 input coupling switch to GND.
   AUTO button out (ON).
   X MAG. button out (X1).
   X shift control (horiz. arrows) to approx. mid setting.
   TIME/DIV switch to 5μs.
   A horizontal trace should appear on the screen as the INTENSITY control is advanced.

3. Adjust the INTENSITY control to obtain a display of the required brightness.

4. Adjust the FOCUS control to obtain a sharply defined trace.

5. Adjust the CH1 Y shift control and the X shift control to centralise the trace on the screen.

6. Adjust the TRACE ROTATE preset control if necessary to align the trace with the centre graticule line. It may be necessary to re-adjust this control only when the instrument is re-positioned as the beam deflection can be affected by earth's magnetic field or other sources of magnetic radiation.

7. Adjust the TIME/DIV switch to 5ms/div, switch to STORAGE mode, and select x1 X-expansion. A power up message will appear at the bottom of the screen. This displays the version of the software fitted in the instrument, and the RS423 default baud rate (see sect. 3.9.2 for details of setting it up).
   eg. "Vers 1.0 BR = 1200"
   The presence of this message shows that the initial power-up tests have been successful. Pressing the On/Off cursor button removes this message, and replaces it with the normal cursor measurement display. Switch back to NORMAL mode.

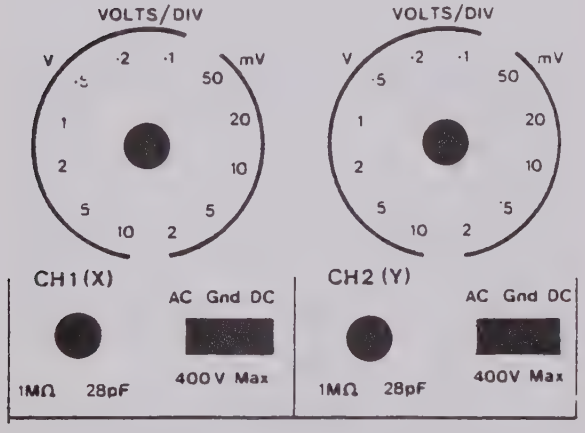
NOTE: The 1425 should not be operated close to sources of alternating magnetic field such as large transformers as these may interfere with the trace.

3.3 SETTING UP THE Y CHANNELS

1. Using a coaxial input signal lead, connect a signal to the CH1 or CH2 input socket.
2. For
   (a) Direct connection of the input signal set the associated AC–Ground–DC slide switch to DC.
   (b) Capacitative coupling of the input signal through an internal 0.1μF 400V capacitor, set the slide switch to AC.

NOTE: When examining low amplitude a.c. signals superimposed on a high d.c. level. the slide switch should be set to AC and the sensitivity of the Y amplifier increased as in (4).

3. To locate the base line, set the slide switch to the GND setting. At this setting, the input signal is open circuit and the input to the amplifier is connected to ground.



4. To select sensitivity, set the VOLTS/DIV switch to the required range. For calibrated operation, the VARiable sensitivity control should be set fully clockwise to the CAL position. This control can be used however to reduce the gain of the relevant amplifier and obtain any intermediate sensitivity between the calibrated switched ranges. To set to any particular calibrated sensitivity, the actual variation from the calibrated range can be set by viewing the CAL 1 Volt o/p on the 0.1V/cm or 0.2V/cm ranges. If the VAR control is not moved, the sensitivity will differ from the calibrated value by approximately the same proportion on all settings of the VOLTS/DIV switch.

   To minimise pick-up at sensitive settings, it is essential to ensure that the ground lead connection is near to the signal point.

5. For vertical movement of the trace, adjust the Y shift controls (identified by the vertical arrows).

6. Any trace movement under no-signal conditions, when the setting of the VOLTS/DIV switch is altered, can be overcome by adjustment of the relevant preset front panel balance control.

   This control will only need adjustment at infrequent intervals. Before adjusting the BAL control, however, ensure that the input coupling switch is set to GND.

   No adjustment should be made until a minimum of 15 minutes warm-up time has elapsed after switch-on, or immedately after any large change of ambient temperature.

3.4 DISPLAY MODES

The mode switch determines the form of the display. In the STORE mode some of the display modes are not available. These will be indicated in the relevant paragraph.

3.4.1 SINGLE CHANNEL

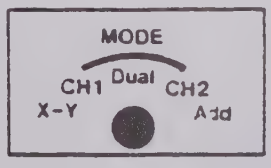
For single trace display of one Y input against the time-base this switch should be set to CH1 or CH2 and the input signal applied to the appropriate input connector.

3.4.2 DUAL CHANNEL

For dual trace simultaneous display of both Y inputs against the timebase, this switch should be set to DUAL.

In the NORMal operating mode, two modes of beam switching are used and are selected automatically by the sweep rate selected by the TIME/DIV switch. The alternate mode is used at fast sweep rates between 0.2ms/div and 0.5μs/div. At the slower rates from 0.2s/div to 0.5ms/div the chop mode operates at approximately 500kHz.

In the STORE mode the display is beamswitched alternately at a fixed rate of 200Hz.



3.4.3 ADD

In the ADD mode, which is only available in the NORMAL operating mode, the single trace generated against the timebase is the algebraic sum of the CH1 and CH2 deflections.

If the INV CH2 button is operated the direction of the Y deflection for that channel is reversed. If used in the ADD mode, this facility allows the difference between the CH1 and CH2 inputs to be displayed. The INV CH2 button has no effect on the polarity of internal CH2 trigger.

When examining small differences between large signals, the effects of small errors between the sensitivities of the

two channels can be overcome by first connecting one input to both channels simultaneously and adjusting one or other of the VARiable sensitivity controls to obtain a straight line.

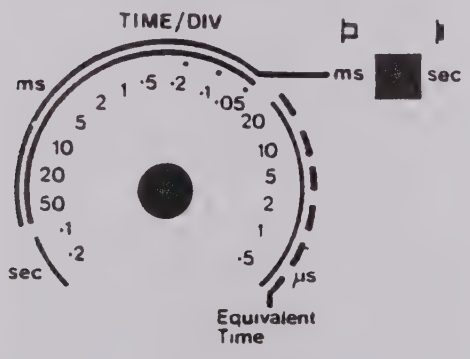
In the STORE mode, the ADD position of the MODE switch is equivalent to the CH2 position.

3.4.4 X–Y

In the X-Y mode, which is only available in NORMAL operating mode, the timebase is disabled and the CH2 input is delayed as the vertical Y deflection against the CH1 input displayed as horizontal X deflection. The CH1 shift control is inoperative and X position is determined only by the X shift control. The X10 MAG facility is also inoperative. X deflection sensitivity being determined by the CH1 controls only. The X bandwidth is limited to 1MHz and relative phase shift between X and Y deflections may exceed 3° above 50kHz.

In the STORE mode selection of X-Y is equivalent to the selection of CH1.

3.5 TIMEBASE AND X-EXPANSION

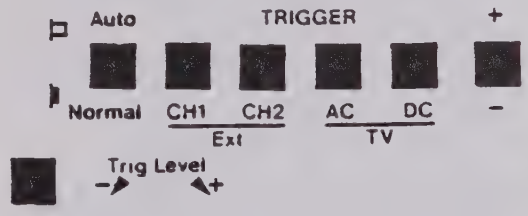


The calibrated sweep speed of the internal timebase is determined by the setting of the TIME/DIV switch and additionally in STORE mode by the ms–s button. When this button is in, the milliseconds section of the TIME/DIV switch is converted to seconds, for example 1ms/div becomes 1s/div. In NORMAL operation and in STORE mode on the SAMPLING section of the TIME/DIV switch, the sweep rate may be varied by the VARiable SWEEP control, enabling intermediate sweep rates between the calibrated ranges to be obtained.

For horizontal shift of the trace, adjust the X shift control (horizontal arrows). If close examination of any portion of the trace is required, X10 expansion can be introduced by operation of the MAG Button. This provides an effective trace length of 100div and any portion of this may be selected for viewing on the screen by operation of the X shift control.

3.6 TRIGGER

The timebase may be triggered internally from the CH1 or CH2 signals by operation of the corresponding TRIGGER button, irrespective of whether the selected channel is being displayed. Alternatively, the timebase may be triggered from an external signal applied to the EXT TRIG sockets when both CH1 and CH2 buttons are operated simultaneously.



The + – button selects the slope, positive or negative going, which causes triggering when the signal passes through the level set by the TRIGGER LEVEL control. Presence of a TRIGGER signal is indicated by the associated TRIGGER l.e.d. This will flash at low trigger repetition rates and remain on at faster rates. Normally triggering can be obtained from internal deflection signals greater than 0.3div pk/pk up to about 2MHz but the sensitivity reduces to about 1 div pk/pk at 20MHz. Corresponding external sensitivity is 0.25V pk/pk to 2MHz and 1.25V pk/pk at 20MHz.

With AC coupling, the low frequency sensitivity reduces to 1 div pk/pk at about 2Hz.

The Ext Trig input impedance is approx. 100kΩ/10pF and care should be taken not to apply more than 250V d.c. or pk, a.c. to this socket.

When the AUTO button is out or ON, the timebase will free run in the absence of a correct trigger signal, to display a bright line or unsynchronised display until the level control is adjusted and/or the amplitude of the trigger signal is increased. This free-run action in the absence of correct trigger, helps in finding the trace and leads to ease of operation. If the timebase is required to free-run continuously, the LEVEL control should be set to either end of its rotation.

It is expected that the NORMAL mode will be selected only when the instrument is to be used to display signals as repetition rates less than 40Hz or faster than 2MHz. This will prevent additional free-run sweeps from occurring between correctly triggered low frequency sweeps or erratic high frequency operation.

The coupling of the trigger signal may be selected as a.c. or d.c. by operation of the corresponding TRIGGER button. When both are pressed, an active synch. separator circuit is introduced to provide line or frame triggering for video waveforms. Field trigger occurs at low sweep rates up to 100μs/div and line trigger is automatically selected at fast sweep rates from 50μs/div. The trigger polarity should be selected for the polarity of the

synch. pulses. At least 0.3div pk/pk of synch. pulse amplitude is required with internal triggering, or 0.25V with external.

Summarising the use of the trigger controls for most applications:

(a) With Auto (button out), select the trigger source CH1, CH2 or EXT and the coupling required, AC or DC.

(b) Select the trigger slope + or – and adjust the trigger level control to obtain a trace which is triggered at the required point.

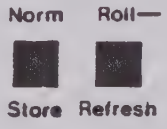
3.7 STORE CONTROL

STORE mode is selected by depressing the NORM/STORE button. The various STORE modes are selected by operation of the buttons on the right hand side of the NORM/STORE control, and by the buttons on the right hand side of the TIME/DIV switch. All controls associated with the STORE mode are labelled in blue.

3.7.1 NORM/STORE

With this button out, NORMal operation is obtained. The instrument behaves like a conventional 20MHz oscilloscope. All controls associated with STORE mode have no effect.

With the button in, STORE mode is selected and the display is produced by the reading out of a digital store. Acquisition of data for this store, and the subsequent display of this data is controlled by the controls labelled in blue.



3.7.2 ROLL/REFRESH

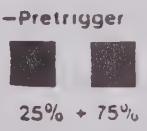
Selection of ROLL provides a form of free running time-base not found on a conventional oscilloscope. Incoming data is fed continuously to the store. As the display is thus updated, the trace appears to be moving or rolling to the left, in appearance, similar to the view through a 10cm window of a strip chart recorder trace.

As information is being continuously written into the store, at a trigger instant the store will only contain pretrigger information. Thus by using the single shot facility (see 3.7.3, 3.7.5) pre-trigger information even for transient signals may be stored and displayed.

The rate of rolling is controlled by the TIME/DIV switch and ms–s button. At high roll speeds the display becomes meaningless to the user, so for the top three ranges of roll mode, 0.2ms/div, 0.1ms/div, 0.05ms/div, the display is blanked while information is stored in the memory. Once the information has been acquired ready for display, the store is read out once, and then, if release mode has been selected, the store is again updated and the display again blanked; the cycle of acquisition then display repeating until an alternative mode is selected. If trigger signals are not present and Auto is off the display will be blank on these three ranges until a trigger signal is present. The display on these three ranges still has a pretrigger facility in the released roll mode. Roll mode can be used on ranges 50sec/div up to 0.05ms/div.

If REFRESH is selected, the display obtained is similar to that obtained on a conventional oscilloscope but with the advantage of flicker-free operation at low timebase speeds. The display updates from the left hand side of the screen on receipt of a trigger as in conventional operation. If the instrument is in single shot mode (see 3.7.5) or the trigger is not present the display retains indefinitely the information captured on the previous sweep until a trigger is received in released mode or the instrument is rearmed. On the top three ranges of the TIME/DIV switch for which refresh is applicable. 0.2ms/div, 0.1ms/div, 0.05ms/div, the display is blanked while the store is filled and then read out once when the acquisition is complete; this cycle repeating if in released mode, or if in single shot mode readout is then continuous. As in roll mode the display will be blanked if a trigger signal is not present, unless the display has been held or restored. Refresh mode is only used on ranges of 50s/div to 0.05ms/div of the TIME/DIV switch.

3.7.3 PRETRIGGER/25% + 75%

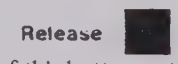


These two buttons select the amount of pretrigger required when using the Roll mode single shot facility (see 3.7.2 and 3.7.5). With both buttons out, 0% PRE-TRIGGER is selected, with only the 25% button depressed 25% PRETRIGGER is selected, similarly for the 75% button, and with both buttons depressed 100% PRETRIGGER is selected.

The amount of pretrigger selected determines the percentage of the display which is acquired before the trigger point, and hence the position of the trigger point on the display. For example, if a trace is stored with 25% Pretrigger selected, the trigger point is 2.5div from the left hand side of the display, the first 2.5div of the display is pretrigger information, and the last 7.5div is posttrigger information.

Pretrigger as mentioned earlier is available in the roll single shot mode, but on the three top ranges of the TIME/DIV switch for which roll is available, 0.2ms/div, 0.1ms/div and 0.05ms/div, the pretrigger facility is available in the released roll mode also (see 3.7.2 and 3.7.4). On these ranges a 'refresh' type display is obtained but with the position of trigger point being selected by these buttons.

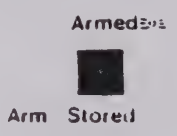
3.7.4 RELEASE



Operation of this button puts the instrument into its continuous acquisition mode. In ROLL this means that the display 'rolls' continuously and ignore triggers except on the ranges 0.2ms/div, 0.1ms/div and 0.05ms/div (see 3.7.2). In REFRESH the display updates until the display is filled with new information and then updating ceases until a trigger is received. The display will again begin updating from the left hand side of the screen. This cycle of refreshing the display, then awaiting a trigger, repeats indefinitely in the released refresh mode.

Release has a different function in timebase ranges of 20μs/div to 0.5μs/div. The scope only works in single shot mode (see section 3.7.5) in these ranges and once armed the timebase switch is ignored until the scope is stored, unless the release button has been pressed.

3.7.5 ARM



This button when operated initiates the single shot storage facility of this instrument. On arming, in ROLL mode, the trace will roll across the screen, and the ARMED/STORED l.e.d. will begin flashing.

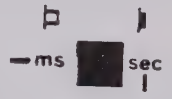
When a trigger is received the l.e.d. will cease flashing and switch off. Meanwhile the trace continues rolling, and after the required amount of pretrigger information is obtained, the instrument will accept a trigger, and when the required amount of post trigger information has been acquired the trace will cease rolling and the ARMED/STORED l.e.d. comes on continuously. The display will not now alter unless rearmed, or put into release mode by operating the release button. In refresh, operation of the ARM button stops the display updating if currently occurring and initiates flashing of the ARMED/STORED l.e.d. On receipt of a trigger the display will begin updating from the left hand side of the screen and the l.e.d. will cease flashing. When the display has been fully refreshed the STORED l.e.d. will come on. This display will now not alter unless rearmed or released.

In this single shot mode of operation there is an extra facility, Equivalent Time SAMPLING, available on timebase ranges 20μs/div to 0.5μs/div. By using a repetitive sampling method it is possible to digitise waveforms which are repetitive in nature, up to the full bandwidth of the oscilloscope. Operation of ARM will blank the previous display and initiate a store cycle.

The store is then updated, one store location per channel per sweep of the timebase. During this process a dot is displayed which moves across the screen as the store is filled. Lack of triggers will cause the dot to halt and the TRIGGER l.e.d to extinguish until triggers are again present. Once the store is full the stored l.e.d. will come on and a display of the stored waveform will occur until rearmed.

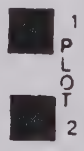
Note that PLOT1 and PLOT2 will always perform a digital plot in these timebase ranges (see section 3.7.7.2).

3.7.6 ms—s



When this button is out the TIME/DIV milliseconds ranges remain correct. However, when the button is depressed this multiplies the TIME/DIV millisecond ranges by one thousand converting the millisecond/cm ranges to second/cm. It has no effect on other timebase ranges.

3.7.7 PLOT 1 PLOT 2



Both analogue and digital plot outputs are available on the 1425 and they are selected by means of the DIL switch (SW1) mounted internally on the CPU board. Analogue plot is chosen by setting posn 3 of the DIL switch to OFF (default position on leaving factory) and digital plot by setting it to ON.

A plot can only be initiated if the display is STORED (see 3.7.5) or DISPLAY HOLD is operated (see 3.7.8). If the trace is not held or stored then a warning message will be displayed:—

"NOT STORED YET"

3.7.7.1 ANALOGUE PLOT

Once selected then pressing PLOT1 will initiate a plot of CH1 and similarly PLOT2 a plot of CH2. The plot X and Y outputs are on the rear panel of the instrument. A penlift signal is also available which is an open collector TTL o/p that goes high to indicate a pen lift is required.

Analogue plot can only be initiated if the TIME/DIV switch is set in milliseconds/cm range. The plotting speed is then one-thousandth of the TIME/DIV range selected, for example a selection of 0.2ms/div on the TIME/DIV switch gives a plotting speed of

1/0.2 * 1000 div/ms which is 5div/s.

NOTE: When plotting a trace captured on 50μs/div in dual channel mode, plot rate will be twice that indicated by the timebase switch.

To abort an analogue plot, press the RELEASE or a PLOT button. Note this will cause the plot rate to increase to the maximum rate of 50ms/div before the penlift occurs.

3.7.7.2 DIGITAL PLOT

Digital plot is chosen by setting to on posn. 3 of the DIL switch on the CPU board. Once selected then pressing PLOT1 will initiate a plot of CH1 and similarly PLOT2 a plot of CH2. The output is from the RS423 socket on the rear panel, in a form suitable for a number of digital plotters with RS232 interface options (including Gould and HP plotters). The format used is HPGL, and an example is shown below.

To abort a digital plot, press either PLOT button.

A box is drawn, with ticks along its edges for calibration. A label at the top shows the attenuator and timebase settings at which the store was captured with a label at each end of the trace. Note that a CH1 digital plot produces its label at the top left, but a CH2 digital plot produces its label at the top right. This means that if CH1 and CH2 are both plotted on the same sheet of paper, the labels are not confused. If the digital plotter used has the capability for different colour pens, a different pen will be used for each channel, so that the two traces can be distinguished. At the end of each plot an overall graticule can be plotted as the full graticule lines (10 DIV x 8 DIV). The alpha numeric display will indicate

"SET DATUM = GRAT"

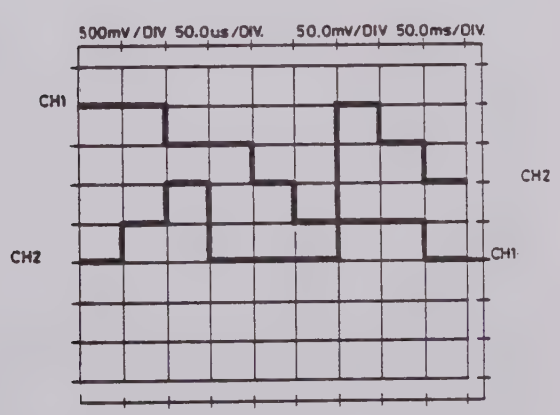


FIG. 12a

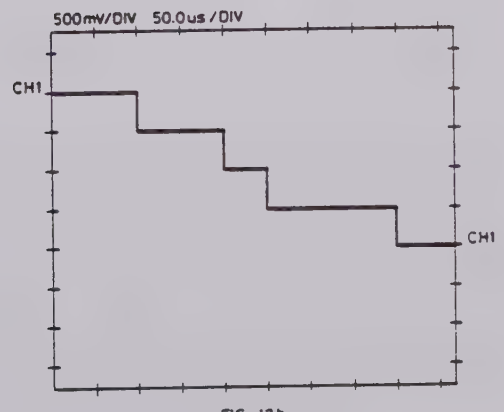


FIG. 12b

If not required the next operation of a cursor button will cancel the display.

NOTE: THE START OF TRACE IN PLOT WILL ALWAYS BE AT THE LEFT HAND GRATICULE LINE IRRESPECTIVE OF THE X POSITION CONTROL.

3.7.8 DISPLAY HOLD

Operation of the HOLD–ALL freezes the display so that no further modification of the display can occur.

It can be used in ROLL mode to freeze the display if a feature of interest appears on the screen. Alternatively it can lock the display in REFRESH mode. Once the trace is frozen it can be plotted using PLOT 1 or PLOT 2 as required.

When the button is released, the instrument returns to a RELEASE mode. Hence operating HOLD will clear an ARM condition.

Operation of the HOLD–CH2 button freezes CH2 data but allows continued updating of CH1, providing comparison facilities between CH1 and CH2. On the 0.2, 0.1 and 0.05ms/div timebase ranges the trace will move in X, moving the trigger point of the held CH2 waveform.

It should be noted that movement of the function switches after a display has been locked can disturb the display, particularly shifting the start point of the trace.

3.8 CURSOR MEASUREMENTS

3.8.1 THE CURSORS

The measurement system is based around the difference between two samples on a trace. The positions of the two samples are shown on the display by cursors, a small vertical line centred about the trace in question and a datum. The datum is shown by a dotted vertical line the full length of the screen. The main cursor and the datum can be moved to a required position on the trace using the five buttons under the screen. The main cursor can be moved left and right at will, and the datum line stepped to its current position using the Set Datum button. The main cursor can then be repositioned

relative to the datum. The display at the bottom of the screen shows the difference between the two sample points on the trace, as pointed to by the main cursor and the datum line.

The buttons are:

On/Off to turn the cursors and the character display on and off.

CH1/CH2 to change the cursors between the traces. Pressing this button moves both cursors from one trace to the other, and the display shows the voltage and time difference between cursors on that trace.

Set Datum Moves the datum line to the current horizontal position of the main cursor. To move the datum line, the procedure is to first move the main cursor to the required position, and then push the Set Datum button.

Cursor left cursor right These two buttons move the cursor in the required direction. If pressed quickly then only one dot is moved. If held down, the cursor moves slowly for a short time, pauses briefly then moves quickly.

3.8.2 THE DISPLAY

The 16 character display at the bottom of the screen is only visible under certain conditions.

a) The instrument must be in a Storage mode (ie either Refresh or Roll)

b) x10 X-expansion must not be selected.

The display screen consists of 16 characters at the bottom of the screen. As mentioned in section 3.2, a message appears on power up, confirming a successful power up sequence. Pressing one of the cursor buttons removes that message, and the display is dedicated to cursor measurements, showing the voltage and time difference between the main cursor and the datum.

An example of the cursor measurement display is:

"CH1–4.45 V 1.234ms"

As shown the information is in three sections:
channel; voltage difference; and time difference.

The first three characters indicate to which channel the two cursors are allocated, and change between "CH1" and "CH2" as the CH1/CH2 button is toggled. The next 6 characters show the voltage difference between the cursors, and the final 7 show the time difference (ignoring decimal points, which do not occupy a character space).

Note that although these numbers might be displayed to several decimal places, the accuracy of the measurement is limited by the digital sampling technique. See the specification section for its actual limits, samples are accurate to 1 in 256 across the screen vertically of 1 in 25 can be expected. The difference between two samples could be in error by 2 bits (1 bit for each sample), giving an accuracy of 1 in 12 for 1cm signal. Horizontal resolution is 1 in 1024 across the screen giving measurements in 0.1/steps. No account is taken of the Volts variable position therefore the control can be used to scale readings but for full calibration ensure the control is switched to the CAL position. In the sampling mode the variable timebase control must be switched to the CAL position for full accuracy.

If the timebase is set to 0.05ms/div, and the 1425 is in dual mode, then there are only 512 dots across the screen, due to speed limitations of the A to D converter.

Note there are some conditions where the display will either not be present, slowly display one channel (without alpha numerics), or be updated infrequently, as follows:–

(a) During an analogue plot.

(b) Whilst acquiring (ie. the scope is armed but not stored) on the timebase ranges 20μs/div to 0.5μs/div (see section 3.7.5) and ranges 0.2ms/div to 0.05ms/div.

(c) When released (not stored or held), and there is a low trigger rate, on the timebase ranges 0.2ms/div to 0.05ms/div.

3.9 RS423 INTERFACE

3.9.1 INTRODUCTION

The interface allows a computer to read from and write over the two stored traces, as well as read the state and change some of the front panel button settings.

A distinction is made between local and remote mode, the scope going remote on receiving a <crlf> terminator from the interfacing computer or terminal. The response to entering remote mode depends on the baud rate chosen, the display only being updated at the lowest baud rate (see 3.9.4). At all baud rates the cursors are switched off and the cursor controls have no effect, apart from the on/off button which returns the scope to local. When remote, the remaining front panel controls can still be operated, the timebase reverting to the range chosen, if it is manually adjusted.

ON GOING REMOTE, IT IS NECESSARY TO WAIT 1 SECOND BEFORE SENDING THE FIRST COMMAND, otherwise it may be ignored.

On returning to local the machine state will return to that selected by the front panel controls, with the exception of ARM and RELEASE. Thus if HOLD had been turned on when remote, but the button indicated that it was off, then the instrument would no longer be held when local. While remote, pressing the HOLD button in and out will also turn hold off.

A command (eg. ST1) can be aborted, by sending 03 (control-C) to the 1425, unless it is a binary transmission of data (ie. command ST1=#B. . . . . .)

Note: In normal mode the scope will not go remote, and if already remote, and it is put into normal mode, it will ignore any further commands until it returns to storage mode.

Errors received by the 1425 are handled on a "Service Request" queue. For details see SRQV section of RS423 commands.

The 1425 interface usually works with full duplex, echoing any characters sent to it. This can cause problems with some computers, so a facility has been provided to turn it off using switch 4 of the DIL switch pack, SW1, on the CPU board. If switch 4 is on echo is on and if switch 4 is off, echo is off.

3.9.2 BAUD RATE SELECTION

The default baud rate is selected by switches 1 and 2 on the DIL switch pack, SW1, on the CPU board (located along the side of the tube), as indicated in the following table:-

Baud Rate	Switch 2	Switch 1
300	OFF	OFF
1200	OFF	ON
9600	ON	OFF
9600	ON	ON

The switch is only read at power up, so to reset the default baud rate the machine must be turned off and on again after changing SW1.

Note: An alternative baud rate can be selected using the remote command "BR=" (see RS423 commands section).

3.9.3 RS423 SYNTAX

A string is the smallest complete message unit.

eg. "HSA=5E-3"

Comma may be used in certain strings as a separator; semi-colon is used to separate strings from each other.

eg. "HSA-5E-3;ST1=1,2,3,4,5,6,7 . . . . . ."

A string should contain only ASCII characters (except when sending in binary), and any control characters, or bytes greater than 127 are ignored. Note that spaces in a string are also ignored.

A BLOCK is a collection of strings. It is merely used in to break up bulk transmissions of stores. Blocks are separated by <crlf>. (Carriage return, line feed).

A RECORD. A record contains a number of strings or blocks and is terminated by <crlf>. The instrument will accept one record into its input buffer before actioning it (excepting store contents, which will overflow the buffer).

When the instrument transmits, it will issue one record for each interrogative command in the record in the input buffer.

Note that when the 1425 is receiving a record, the correct method of termination is <crlf>.

So valid record terminators are:

<record> <crlf>
<record> <lf>

3.9.3.1 OPERATION

The 1425 processes commands sent as ASCII (ISO-7) blocks. The instrument will perform no operations until a record terminator is received (or the input buffer overflows).

Most commands have an interrogative form, and an assertive form.:

eg. "HSA" <crlf> is a request for the current setting of the timebase to be transmitted

while

"HSA=1" <crlf> is a request for the setting to be set to 1sec/div.

In general, several commands can be combined into a, record (each command separated by a semi-colon). The commands will then be actioned in sequence

eg. "ARM;STAT"<crlf> will arm the scope (equiv to Single Capture), then send the status of the scope. Repeated requests for status could be used to find out when a store had been captured.

There are two exceptions to this rule: the bulk transmission commands ("ST1=. . ." and "ST2= . . .") must be the last command in a record. This also applies to the special command "ALL".

3.9.3.2 NUMBERS

Commands that have numeric parameters (eg HSA; horizontal speed) require the number to conform to certain limitations:

1. The number must contain less than 20 characters
2. The number must NOT contain a decimal point (ie it must be an integer).
3. The number can contain, but need not contain a sign ("+" or "–")
4. The number can contain, but need not contain an exponent.
5. The exponent is prefixed by "E".
6. The exponent can contain, but need not contain a sign.
7. The exponent must not contain a decimal point.

Note that bulk data transfer commands (eg "ST1") have more strict syntax requirements. See section 3.9.6.

When the 1425 transmits a number, it will conform to the above requirements, but in addition, the mantissa will be less than 4 digits, and the exponent, if any, will be a multiple of 3, eg "HSA= 500E-3".

3.9.4 THE DISPLAY WHEN REMOTE

"At 9600 baud the alpa-numeric display that normally displays the cursor difference measurement is turned off completely. At 1200 and 300 baud the message

"REMOTE" is displayed, but no further changes will take place unless the TXT command is used (see description of TXT command).

Note: The display has the same limitations as outlined in section 3.8.2. That it is not available in normal mode, with *10 X-expansion selected, and whilst armed or waiting for trigger, in some timebase ranges (see sect. 3.8.2 for details).

3.9.5 THE RS423 COMMANDS

The following is a list of RS423 commands available for the 1425.

ALL

This interrogative command sends out the complete state of the instrument as though all interrogative commands had been sent. Its response is in the form of a number of blocks, separated by <crlf>.

ARM

This assertive command is the remote equivalent of the Arm button on the front panel. Sending this command arms the 1425 trigger circuitry, it waits for the next trigger, and then captures a trace. A service request is generated ("completed") when the trace is captured. If it is not possible to capture a trace (eg because LOCK=ON), then a different service request ("selection failure") is generated.

eg "ARM" capture a single trace.

BL

This command is used to set the block length to be used when sending the contents of the stores (ie ST1 and ST2). Its initial value is 0, and it can have a value between 0 and 80. It specifies the maximum block length that will be sent before sending a <crlf>. The store contents is sent as a list of strings, separated by commas. If the number of characters so far sent is going to exceed the block length, then <crlf> is sent instead of a comma. If the block length = 0, then an infinite block length is assumed, and the only <crlf> sent is the one right at the end of the record.

eg "BL"
"BL=0" (response: block length is 0)
eg "BL=32" set the block length to 32.

BR

This command will display the current baud rate, or allow the baud rate of the scope to be changed remotely. Once used the baud rate of the issuing computer/terminal will have to be changed correspondingly. There are only three possible baud rates to choose from: 300,1200 or 9600. The 1425 will not revert to the default baud rate until it is switched off and on again (see section 3.9.2).

eg. "BR=9600" (changes scope baud rate to 9600 baud)

DC1 DC3

This command is used to turn on or off the XON–XOFF (DC1–DC3) handshake, which controls data coming into the 1425, allowing a three wire interface (Tx, Rx, and ground). The XON and XOFF handshake controlling data from the 1425 is always active (except for binary transfers). The command can also be used interrogatively to indicate whether the handshake is active, (see section 3.9.9 for handshake details).

eg DC1 DC3 = ON
(1425 turns XON XOFF handshake on).

DPLOT 1 and DPLOT2

These commands are the direct equivalents of the RS423 digital plot facilities on the front panel. The response is to send a string for use by a RS232 digital plotter, in HPGL format. The string is extremely long (approximately 8000 characters), and specifies the position of each of the points on the display in terms of its X and Y co-ordinates. See section 3.7.7.2.

Note that because the RS423 interface ignores whether the Y-Variable controls are in the CAL or the UNCAL state, it is up to the operator to ensure that those controls are in the correct position if a calibrated plot is required.

For reference, a possible first 300 characters of a typical output are shown below:

eg "DPLOT1" send out a digital plot string.

(1425 response:)
SP1;SC-2,1024,-130,+133;PU;PA-1,128;PD.PA1024,128,
1024,-129,819,-129;XT.PA614,-129;XT.PA410,-129;
XT.PA205,-129;XT.PA-1,-129,-1,-64;YT;PA-1,0;YT;
PA-1,63;YT.PA-1,128;PU;SL.3;PU;PAO,129;LB
200mV/DIV 5.00μs/DIV PU;PA1,-20;PD.PA2,-30,3,
-33,4,-34,5,-34,6,-35,7,-36,6,-35,9,-35,10,-34,11,-35,12,
-35,13,-35 etc., etc.

HELLO

The response to this command is to send a string containing the current version number of the software in the instrument. The string is in the same format as the power up message on the screen, and also contains the Baud Rate.

eg "HELLO"
"Vers 1.0 BR=1200" (1425 response)

HELP

This command is a request for a list of all available commands. The response is a block containing the currently available commands, separated by semi-colons. Interrogative commands are distinguished from assertive ones by having a "=" appended. Note that the block length command does NOT apply to this command, and the only <crlf> sent is right at the end of the record.

eg "HELP"
"HELP;HELLO;ALL;PLOT;DPLOT1;DPLOT2;
VM;HSA;HSA=;ST1;ST1-;ST2;ST2=;

HOLD2

This command is the equivalent of the HOLD2 button on the front panel and prevents the update of channel 2 from the signal input. In its interrogative form it says if this function is active. In its assertive form it allows or prevents CH2 update. There are two possible parameters "ON" and "OFF". See sect. 3.7.8 for details.

eg "HOLD2"
"HOLD2=ON" (1425 response: CH2 held)

HSA

This command is used to set or read the current horizontal speed (ie. the timebase range). On returning to local, the timebase returns to the range indicated by the timebase switch, if it has been changed using this command. The units used are seconds/division. Note the limitations on acceptable types of number in section 3.9.3.2. The range of possible values is 50 to 5E-7, in a 1,2,5 sequence (ie. 50s/div to 0.5μs/div), with the following limitations on selection:

(a)In normal (non-storage) mode the remote facility is inactive (see sect. 3.9.1).

(b) A timebase speed in the range 20μs/div to 0.5μs/div (the SAMPLING ranges), cannot be selected remotely, unless the timebase switch is set to the range required. Any attempt to do so will result in a SRQ error value to be added to the SRQV queue (see sect. 3.9.7).

eg. If the timebase switch is set to 1μs/div then
"HSA-1E-6" will work.

"HSA=1E-5" will cause a SRQ value to be queued (attempt to select 10μs/div, a sampling range, when timebase switch=1μs/div)

Note any other non-sampling timebase ranges can be selected, the only restrictions being those specified below (sub-sect. (c)).

(c) If the ms/sec button is in (ie. on secs range) then only the timebase ranges 50s/div to 50ms/div can be selected (apart possibly from a sampling range see (b)). Conversly if the ms/sec button is out (ie. on ms range) then only the timebase ranges 50s/div to 50ms/div can be selected.

eg. in secs mode with timebase 5secs/div
"HSA" (interrogative command)
"HSA=5E+1" (1425 response, indicating that timebase is 5secs/div)
"HSA=50E-3" will work (assertive command to 1425).

LOCAL

This is an assertive command to return the machine to local mode (ie. it is equivalent to pressing the cursor on/off button). In order to go remote again just send a <cr>.

LOCK

This command is the equivalent of the Display Hold All button on the front panel, and has the effect of freezing the display. In its interrogative form, it says if the display is currently locked or not. Its assertive form is used, when remote to lock and unlock the display.

It has two possible parameters, "ON" and "OFF".

eg. "LOCK"
"LOCK=ON" (1425 response: display is locked)

NOTE: If the scope is in timebase ranges 0.2–0.05ms/div the LOCK=ON command may take up to 1 second to respond. The response rate depends on the trigger rate, and if after one second no trigger has occurred the routine times out, LOCK is not actioned and a SRQ value of 100 (selection failure) is added to the SRQV queue. If successful then a SRQ value of 74 (completed) is added.

NB

This is the Numeric Base command. It is used to set the format to be used by the interrogative form of the "ST1" and "ST2" commands. It has four possible parameters "BIN", "OCT", "HEX" and "DEC". For more information, see section 3.9.6 Sending and Receiving Stores.

eg "NB=BIN" set numeric base to binary.
eg "NB"
"NB=BIN" (1425 response: base is binary)

PLOT1 AND PLOT2

These assertive commands initiate an analogue plot of the relevant channel, like the front panel buttons. In the same way, it requires a captured or held trace before it will operate (use "ARM" or "LOCK=ON"). If the trace is not stable, a service request value will be added to the queue ("Selection Failure"), and no plot will be started.

To choose the plot rate, the timebase must be set (using "HSA= . . ."), to the required speed, or if the ms/sec button is not set to seconds, 1000 times the plotting speed (so the software will accept it, see "HSA" section). In plot the scope will ignore the ms/sec button and plot at the slower speed. See section 3.7.7.1 for details. As with a manual plot, no plot will begin if the timebase chosen is in the range 20μs/div to 0.5μs/div (sampling ranges).

Note: When plotting a trace captured on 50μs/div in dual channel mode, plot rate will be twice that indicated by the timebase.

While plot is in progress, no RS423 response is possible, and the display will only show a dot corresponding to the point being plotted (no alpha-numerics). When the plot is finished, a service request value is added to the queue ("Completed"). The plot output is from the three 4mm sockets on the back panel.

The plot can be aborted in the same way as a manual plot, by pressing the RELEASE or a PLOT button (the remote REL command will be ignored).

eg. To hold and plot channel 2 at 5 divs/sec, with the scope set to 1ms/div timebase, use the following command sequence:

LOCK=ON;HSA=5E-3 (set HSA=1000*plot speed)
PLOT2;SRQV

When you receive the response from the scope "SRQV=74", the plot sequence will have finished, so reset timebase using

HSA=1E-3

If the capture rate was 1sec/div, use "HSA=5" in place of "HSA=5E-3", to set plot rate.

REL
This assertive command is the equivalent to the release button. Sending it releases the trigger circuit so that it can keep capturing stores, each time it sees a trigger signal.

eg "REL" keep capturing, continuously.

SRQV
This is the Service Request Value command. In response to this command a value of 0 is given if no service requests are queued up. Otherwise, a number (in decimal) corresponding to the Service Request top of queue is given. Repeated use of this command will remove SRQ's from the stack. See section 3.9.7 Service Requests.

eg "SRQV;SRQV;SRQV; send out the first three
"SRQV=96" SRQ values (1425 re-
"SRQV=102" sponse: there were 2
"SRQV=0" SRQ's waiting, one for invalid command, one for syntax error)

ST1 and ST2
These are the block transfer commands for sending and receiving the contents of the display stores. They only work in the Storage modes. They send or receive a series of 1024 values in a number of different bases. See section 3.9.6 for more details.

ST1HS and ST2HS
These interrogative commands have the horizontal speed at which store 1 or store 2 were recorded. They are in the same form as the 'HSA' command. Note that the speed for store 1 could be different from the current timebase range if the store was captured a while ago. The units are sec/div.

eg "ST2HS" what was the t/b range, when store 2 was captured?
"ST2HS=200E-6" (1425 response: it was 200μs/div)

ST1VS and ST2VS
These interrogative commands specify the vertical range (ie attenuator setting) at which the relevant stores were captured. They have the same form as the "VS1" and "VS2" commands. The units are Volts/div.

eg "ST1VS" what was the attenuator setting when store 1 was captured?
"ST1VS=5E+0" (1425 response: it was 5 volts/div).

STAT
This is an interrogative command to find out the state of the stores. It has three possible parameters, "ARMD", "RELD" and "STRD". If in continuous capture (released) mode, the response will be "RELD". If the oscilloscope has just been ARMed, it will say "ARMED". When a store-full is finally received it will say "STRD".

eg "STAT" what is the status?
"STAT=STRD" (1425 response: a single trace has been captured.)

TXT
This is a method of putting a message onto the 16 character display. The syntax required is:

TXT="<string>"
or TXT='<string>'

The string should not be more than 16 characters long, though decimal points do not occupy a space. There is only a limited character set available. Basically, only upper-case letters and numbers 0 to 9 are usable, but a number of other characters have had to be added, including +,-,=,a,b,c,d,e,f,r,s, a micro symbol (value hexadecimal 7D).

eg "TXT='SWITCH CH1 to 5V/DIV' "

VM
This is an interrogative command, which is used to find the Vertical Mode of the scope as set by the mode switch, ie. whether DUAL, CH1 or CH2 has been selected.

eg "MODE"
"MODE=DUAL" (1425 response: both channels selected for display/update)

VS1 and VS2
These interrogative commands specify the vertical scaling (ie the CH1 and CH2 attenuator ranges). The units are Volts/Div, and they take no account of either the invert switch, or the Variable gain control.

eg "VS1" what is the CH1 attenuator position?
"VS1=10E-3" (1425 response: it is 100mV/Div)

3.9.6 SENDING AND RECEIVING STORES

This is an extended description of the various commands and formats available when sending store information to, and receiving store information from the 1425. It does not include the DPLOT1 or DPLOT2 commands.

The format used for sending store contents is the same as for receiving. So a record previously read from the 1425 can later be sent back, without modification, to restore the display to its original state. However, ensure that data is not being captured while sending a store to the instrument, or the information received will be immediately corrupted (eg send "LOCK=ON" before sending the "ST1- . . ." command).

When the instrument outputs mass data, the numeric base and the block length will be as specified in separate commands by the user (ie "NB=" and "BL=").

When mass data is sent to the instrument, the numeric base is deduced from the data string, and the block length is irrelevant.

MASS DATA TRANSFER DATA FORMAT
Mass data consists of three main sections:

1. A header which is specific to the command in operation (ie "ST1=" or "ST2=").

2. A numeric base identifier (where appropriate):
   ie #B for binary
   #O for octal
   #H for hexadecimal
   If there is no identifier, the base must be decimal.

3. The data itself.
   The data represents a value between -128 and +127 (when numeric base is decimal, or between 0 and 255 for other numeric bases). -128 is below the bottom of the screen, 0 is the middle of the screen, and +127 is above the top of the screen. The nominal step size is 0.035 divisions per step, so to calculate the voltage difference between two samples, ya and yb:

$$\text{Voltage Difference} = (yb\text{-}ya)\ \frac{(\ 35\ )}{(\ 1000\ )}$$

   (attenuator range in Volts/div)

The data is sent as 1022 numbers in the appropriate base. Each base will be treated separately, because they each have their own special features.

BINARY

Sending data in this format is the quickest method. The string is 1034 bytes long (including the <crlf>), in the following form:

ST1=#Blldddddddddddd . . . . . dddddcc<crlf>

Where:

#B is the binary identifier

ll is a two byte count of the following data, up to and including the two byte checksum. Most significant digit first. So the value of "ll" is hexadecimal 0400 (decimal 1024).

ddd . . ddd are the 8 bit binary digits (value 0 to 255) representing the data.

cc is a two byte checksum of the preceeding data not (including the length "ll". Most significant digit is sent first.

If an invalid length is received, a service request is sent ("length error") and the command is aborted. If the checksum is calculated to be wrong, a service request ("checksum error") is sent, but the store has already been received, so it is not very important.

The following programme in BASIC should build up a string that could be sent to the 1425, so as to display four ramps on the screen.

DECIMAL

A string of variable length is sent. It consists of the header "ST1" or "ST2", followed by 1022 decimal numbers, separated by commas, or <crlf>. The numbers are in the range –128 to +127, producing zero for centre screen, and 127 for the top of the screen. Leading zeros are not output, but are accepted. Leading "+" is not sent, but is accepted. No decimal point is accepted, nor is an exponent field.

Values are normally separated by comma, but <crlf> is substituted if the length of the block would otherwise exceed the block length set by the "BL" command. If

```
 10    DIM AS[1500]
 20    C = 0                          REM INITIAL VALUE OF CHECKSUM
 30    A$="ST1=#B"
 40    A$=AS & CHR$(4) & CHR$(0)      REM THE HEADER & IDENTIFIER
 50                                   REM AND THE LENGTH
 60    FOR I = 0 TO 1021              REM MAIN LOOP
 70    X = I MOD 256                  REM DATA TO BE SENT
 80    A$ = A$ & CHR$(X)              REM APPEND THE DATA
 90    C = C + X) MOD 65536           REM UPDATE THE CHECKSUM
100    NEXT I
110                                   REM END OF MAIN LOOP
120    A$ = A$ & CHRS (C DIV 256)     REM APPEND THE CHECKSUM
130    A$ = A$ & CHRS (C MOD 256)     REM Not really necessary!!
140
150    A$ = A$ & CHRS(13)             REM APPEND <CRLF>
160    A$ = A$ & CHRS(10)
170
180        REM NOW SEND THE WHOLE OF AS OVER THE RS423 INTERFACE
```

Block length is zero (its initial value) then a <crlf> is only sent right at the end of the record. Block length can be used to ensure a neat print out on a printer, or for a computer that can only accept limited length strings.

When receiving the information, the 1425 treats commas and <crlf> as the same. So if necessary, each number could be separated by <crlf>.

OCTAL

A fixed length record is sent (4101 characters, including the <crlf>, if BL=0), consisting of the header "ST1=#0", followed by 1022 three character octal numbers. The numbers are unsigned, in the range 000 to 377, with 000 being the bottom of the screen. The numbers are separated by commas, or <crlf>, as for DECIMAL. Leading zeros are sent, but are not necessary when receiving the data.

HEXADECIMAL

A fixed length record is sent (3077 characters, including the <crlf>, if BL=0), consisting of the header "ST1=#H", followed by 1022 character hexadecimal characters. The numbers are unsigned, in the range 00 to FF, with 00 being the bottom of the screen. The numbers are separated by commas, or <crlf>, as for DECIMAL. Leading zeros are sent, but are not necessary when receiving the data.

3.9.7 SERVICE REQUESTS

To handle errors and to indicate when a requested action is completed the 1425 keeps a "service request" queue. Service request values (SRQV's) can be removed from this queue and read by the interrogative command "SRQV". Up to 10 SRQ's can be queued after which a SRQ value indicating queue overflow is added to it. The meaning associated with the various SRQ values is given in the table below.

SRQ value	Meaning to
0	SRQ queue empty
74	completed
96	invalid command
98	SRQ queue overflow
99	buffer overflow
100	selection failure
101	not ready yet
102	syntax error
103	number out of range
104	length error (for "ST1-")
105	checksum error (for "ST1=")

Eg. To capture and transfer CH1, send the command sequence

"ARM;SRQV"

and when the response

"SRQV=74" is received (indicating capture complete), then send the command "ST1" which will transfer the contents of channel 1 (see sect. 3.9.6).

OPTIONAL WAVEFORM PROCESSOR COMMANDS

If the optional Waveform Processor 125 upgrade is fitted to the 1425, then many of its commands will also be accessable via the RS423 interface. See instruction booklet provided with it for details.

3.9.8 RS423 SUMMARY

There follows an alphabetical list of available commands, and a brief description of their use.

Command	Parameter	Command	interrog form	assertive form
ALL		status summary	yes	
ARM		single capture		yes
BL	<number>	block length	yes	yes
BR	<number>	baud rate	yes	yes
DC1DC3	ON OFF	Turn On/Off XON-XOFF handshake	yes	yes
DPLOT1) DPLOT2)		digital plot	no	yes
HELLO		version number	yes	
HELP		list of commands	yes	
HOLD2	OFF	lock ch2	yes	no
HSA	<number>	horizontal speed	yes	yes
LOCAL		leave remote		yes
LOCK	ON) OFF)	lock display	yes	yes
NB	<number>	numeric base	yes	yes
PLOT1) PLOT2)		analogue plot	no	yes
REL		continuous capture	yes	yes
SRQV	<number>	service request value	yes	no
STAT	ARMD STRD RELD	store status	yes	no
ST1)) ST2)	depends on "NB" & "BL"	store contents	yes	yes
ST1HS	<number>	st1 horiz speed	yes	no
ST1VS	<number>	st1 vert scaling	yes	no
ST2HS	<number>	st2 horiz speed	yes	no
ST2VS	<number>	st2 vert scaling	yes	no
TEST	WRITE READ LINES PORTS	various test facilities	no	yes

TXT or	'<string>' "<string>"	display a string	no	yes
VM	CH1) CH2) DUAL)	vertical mode	yes	yes
VS1	<number>	ch1 attenuator	yes	no
VS2	<number>	ch2	yes	no

3.9.9 RS423 HANDSHAKING AND HARDWARE

"There are two handshakes implemented on the RS423, interface, XON–XOFF (commonly known as DC1–DC3) and CTS–RTS. Only the CTS–RTS handshake will work with the transfer of data in binary format.

(a) XOFF–XON (DC1–DC3)
If the 1425 receives the XOFF control code (=19) any further transmission will stop. It will resume on receipt of a XON control code (=17). The same handshake can be enabled in the opposite direction, such that when the 1425 cannot receive data or commands (such as during an analogue plot), it will send an XOFF control code to the host system, followed by an XON code when ready to receive again. This is enabled using the DC1–DC3 command (see section 3.9.5). The machine powers up with the output handshake disabled.

Note if involved in a binary transfer of data, then this handshaking is suspended, as incoming data may include these codes!

(b) CTS–RTS
This is a hardware handshake based on the signals Clear To Send (CTS), actioned by the host, and Ready to Send (RTS), actioned by the 1425. When the host system is ready to receive, it asserts the 1425's CTS line. When the 1425 is ready to receive, it asserts the 1425 RTS line. If the 1425 wants to prevent further transmission from the host (such as during an analogue plot), then it will take its RTS line inactive (low). Similarly, if the host system wishes to stop the 1425 transmitting then it will take the 1425 CTS line inactive (low).

Note: If the CTS-RTS handshake is not available from the host, then the 1425 CTS and RTS lines (pins 4 and 5 of D-type connector) MUST be joined together, in order for the interface to work.

The RS423 connector used is a standard 25 way D-type connector with the following pin-out.

pins 1, 7, 9	= ground
pin 2	= Tx transmit output FROM scope.
pin 3	= RX receive input TO the scope.
pin 4	= RTS "ready to send" signal-active high when scope ready to receive.
pin 5	= CTS "clear to send" signal-active high when interfacing device ready to receive.

The RS423 data format is:

8 bit word with no parity
1 start bit
1 stop bits

3.9.10 RS423 vs RS232

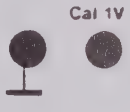
Although the RS423 driver output of 4–5 volts does not meet the RS232C specification of 6 volts, operation is normally satisfactory. This is due to the lower source impedance of the RS423 driver, which means the RS232 receiver input spec. of 3 volts will be met. If used with an RS423 interface (such as on the BBC micro-computer), then much longer cable lengths can be used than with RS232 – up to 2000ft.

3.10 ADDITIONAL FACILITIES

1. Calibrator

The output pin on the front panel provides a positive going 1V flat topped squarewave at approx. 1kHz. It can be used to check the sensitivity of the instrument or to obtain any particular calibrated sensitivity (see section 3.3.4). The rise time is 2μs approx. and the output impedance is 470R providing 2.3mA approx. to ground.

The CAL output may be used to set up passive probes.



2. Z Mod

The socket on the rear panel allows modulation of the bightness. The input is d.c. coupled into approx. 10k/10pF. The sensitivity at normal brightness setting requires approximately 2V to provide visible modulation. 15V is required to obtain a full trace blanking.

Care should be taken not to apply more than 100V d.c. or pk a.c. to this socket.

3. Use of the Passive Probe

A X10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input resistance of a Y channel is 10M ohms, shunted by approximately 28pF. The effective capacitance of the input lead must be added to this and the resultant impedance can often load the signal source. Therefore it is advisable to use a 1M ohms, X10 probe such as PB12 or PB13. This reduces the input capacitance and increases the input resistance, at the expense of a 10X reduction in sensitivity. The probe inserts a shunt RC network in series to form a 10:1 attenuator with the input RC of the Y channel. To obtain a flat frequency response it is necessary to adjust the capacitance of the probe to match the input capacitance of the Y channel as follows:

1. Set the Y channel VOLTS/DIV switch to 20mV, the TIME/DIV switch to 500μs and trigger from the appropriate channel.

2. Connect the probe to the CAL socket.
3. Adjust the probe compensation to obtain a level trace, i.e. flat top without overshoot or undershoot.

4. Camera
A camera may be used with the oscilloscope to record waveforms. This facility is particularly useful at slow timebase sweep rates. Suitable camera utilising Polaroid film may be obtained from Shackman and hand held against the tube face. Other oscilloscope cameras may be used but suitable adaptors must be obtained and should be discussed with the camera manufacturer.

5. Line output
Provided on a rear panel BNC socket, is a line output signal, with a nominal output of 1V peak to peak. The output impedance is 100kohms providing a useful signal for triggering on, when observing mains related events.

6. Waveform processor interface
A second BNC socket exists on the rear, which is used to connect to an optional waveform processor. This provides a range of digital signal processes, plus backup memory (for details see end of specification). In order for this to work, an upgarde kit must be fitted to the 1425 which is supplied along with the waveform processor if ordered separately.

4.0 COMPONENT LOCATION

To aid component location, circuit references have been allocated in the following general pattern.

1 – 99	Components not mounted on printed circuit boards.
100 – 199	Components mounted on the attenuator assemblies.
200 – 299	Pre-Amplifier and Ramp Generator components mounted on the daughter board.
300 – 399	Y Pre-amplifier and Beam Switch components mounted on the main board.
400 – 499	Y amplifer and Y Output amplifier components mounted on the main board.
500 – 599	Timebase and X Output amplifier components mounted on the main board.
600 – 699	Trigger circuit components mounted on the main board.
700 – 799	Power supply and modulation circuit components on the main board.
800 – 999	Digital Storage and Interface board.
1100 – 1199	Function switch board and associated components.
1200 – 1299	Auxiliary Power supply board and associated components.
1300 – 1399	Analogue pick-off board and associated components.
S1400 – S1499	Plot Switch board only.
1400 – 1499	Microprocessor board.
1600 – 1699	RS423 communications board.
1700 – 1799	Switch pick-off board.
1800 – 1899	Cursor switch board.

4.1 GENERAL

With the NORMal/STORE button out the instrument behaves as a conventional oscilloscope. Referring to the block diagram (Fig.1A) signals applied to the CH1 and CH2 input sockets pass into their respective attenuators and amplifiers. The VOLTS/DIV switch controls the gain of the pre-amplifier in steps 1.2.5 sequence to cover the ranges from 2mV/div to 0.1V/div and a ÷100 attenuator is introduced before the amplifier on the ranges 0.2V/div to 10V/div.

The Variable Gain control adjusts the amplifier gain to give 1 to 2.5 times reduction of gain on all settings of the VOLTS/DIV switch. The fast electronic beam switch selects either CH1 or the CH2 signal to be applied further and passed to the Y deflection plates of the c.r.t.

A sample of each signal is taken and passed to the trigger switch bank where selection of CH1, CH2 or Ext trig source is made.

The selected signal is amplified and passed to the Schmitt trigger, the output of which clocks the timebase bistable "on". The ramp generator then begins to generate its linear ramp, which, after passing through the X amplifier, is applied to the X deflection plates of the c.r.t. and drives the electron beam linearly across the tube face. A portion of the signal from the ramp generator is fed back to the hold-off circuit, shutting the gate to prevent any further pulses from the Schmitt trigger from reaching the timebase bistable during the ramp period. When the ramp has reached the necessary maximum level, the timebase bistable is reset, and the ramp is quickly returned to its quiescent state. A time-constant in the hold-off circuit retains this signal to inhibit another ramp from being initiated for a short period, until the ramp timing capacitor is discharged fully. Thus a ramp is generated at a rate set by the TIME/DIV switch when the trigger signal reaches a pre-determined level. This ramp sweeps the beam across the c.r.t. face, returns and waits for the next input cycle to reach the set trigger point, so producing subsequent ramps. The timebase bistable is connected to a blanking amplifier whose function is to turn on the electron beam during the sweep and blank it off during the fly-back and subsequent waiting period.

At fast sweep rates for a dual trace display, the TIME/DIV switch automatically selects the alternate sweep mode of control for the beam switch. At the end of each sweep, the signal from the timebase reverses the state of the beam switch bistable, causing alternate displays of the CH1 and CH2 signal on successive sweeps of the timebase. At slow sweep rates, the chop mode is selected, when the chop multivibrator free runs independently, causing the beam to switch or chop between CH1 and CH2 levels during the sweep.

A signal from the multivibrator also blanks the trace during each switching transition. With CH1 or CH2 only selected, the beam switch bistable is held to select that channel only. In the X-Y mode, the bistable is held to select CH2 as the Y deflection signal, while an additional switch diverts the output from the CH1 pre-amplifier to the X output amplifier, as the X deflection signal in place of the normal ramp signal. The blanking amplifier is held in the bright-up state. When TV trigger mode is selected, an additional synch. separator circuit is introduced into the signal path leading into the trigger amplifier.

During Real time operation the microprocessor is put into SLEEP mode.

When the NORM/STORE button is in the instrument becomes a digital storage oscilloscope (see Fig.1B). The output of the Y dot joiner is routed through to the Y output amplifier. Analogue signals from the Y preamp are picked off, buffered, then fed into two sample and

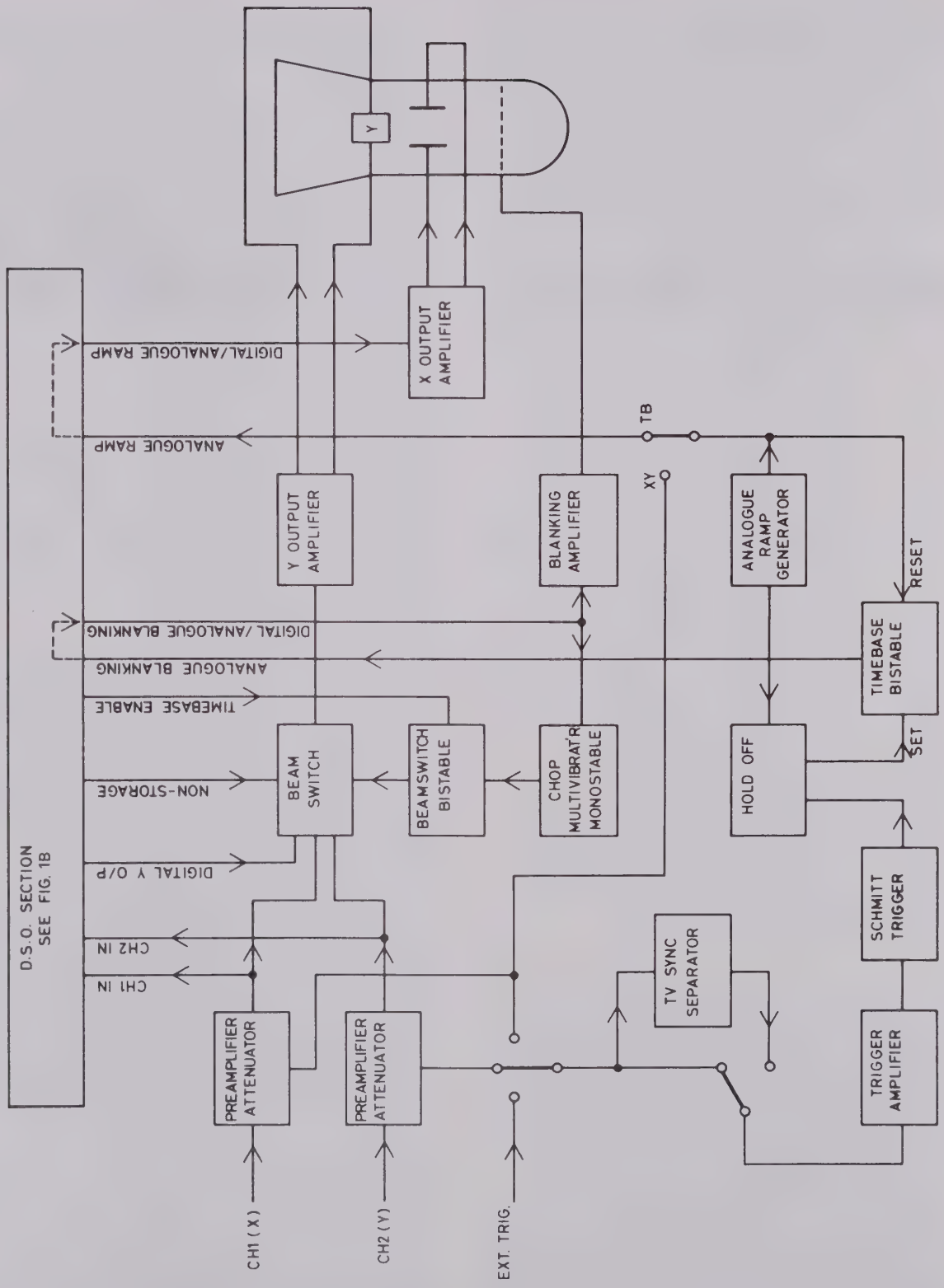


Fig. 1A Block Diagram Real-Time

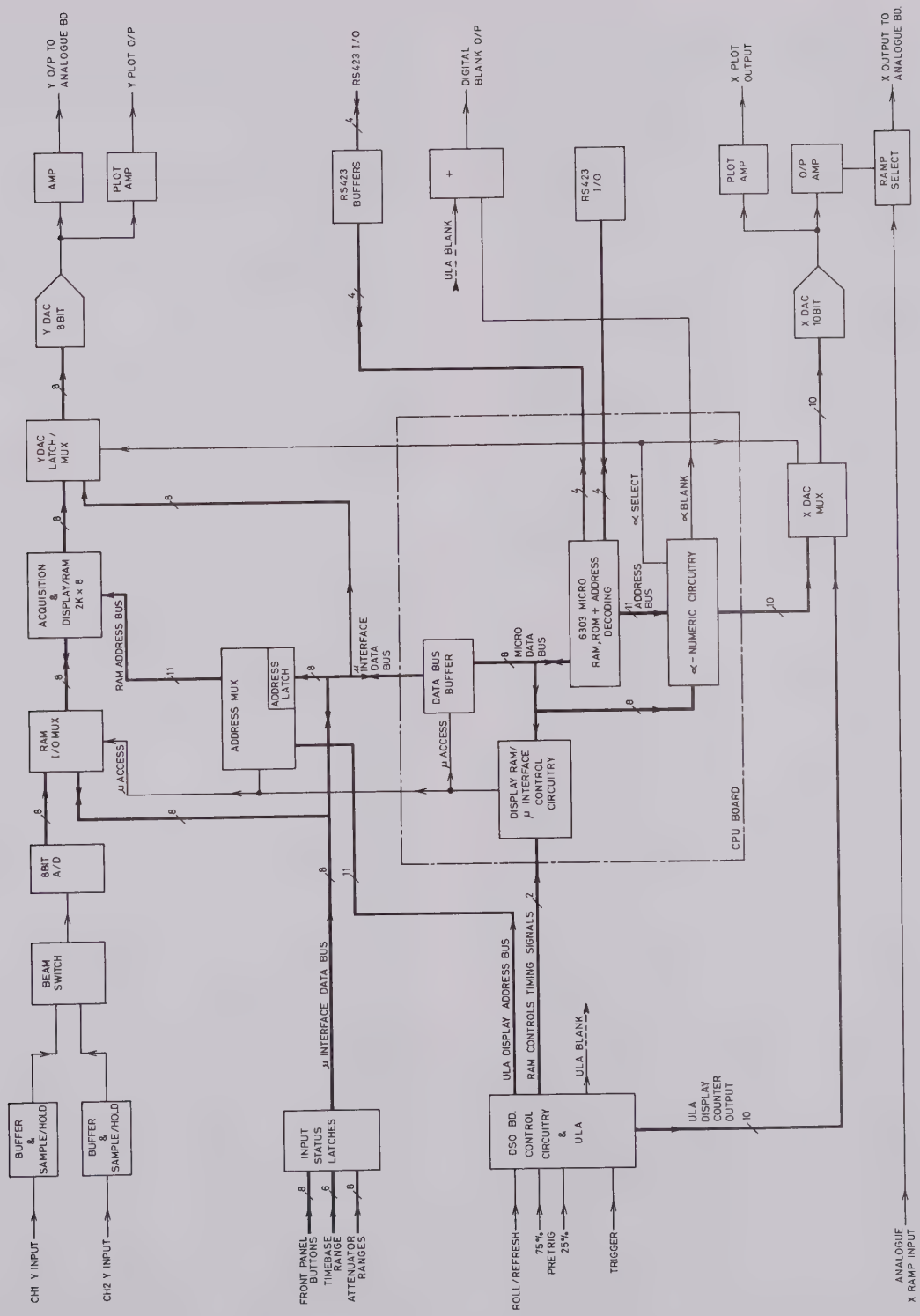


Fig. 1B Block Diagram Storage

hold circuits. The outputs of the sample and holds are beamswitched into the Analogue to Digital Converter (ADC). This produces an 8 bit binary code representing the amplitude of the instantaneous signal input at 500 nanosecond intervals. The data produced is loaded into the store under control of the timing logic. The store can hold 2048 8 bit words and the data is entered at such a rate that the information contained in each of the two 1024 bytes of memory represents one complete sweep of each channel.

The data is then read out (non destructively) at a fixed rate and reconstructed as an analogue signal by the Digital to Analogue Converter (DAC), and applied to the Y output to give a continuous display of the store contents. Since the output of the DAC is in the form of discrete levels a dot joiner is included to join these levels and provide a continuous display.

In all the digital storage modes the timebase sweep is controlled by a ten bit counter which provides an increasing ten bit code which is reconstructed by a ten bit DAC and dot joiner to give an analogue ramp. This ramp is synchronised to the readout of the Y data from the store. This ramp is used to display the two sections of 1024 bytes of store, and during the third display period the microprocessor system provides the X-information to display one line of alphanumerics. This is done sequentially, CH1,CH2,ALPHANUMERICS, if in dual mode or just one section of the store and the alphanumerics if in single channel mode. The trigger is now entirely dissociated from the timebase since the latter runs continuously. The function of the trigger now is, in REFRESH to initiate a write cycle, during which a screen full of new information is entered into the store, and in ROLL to define the amount of pretrigger and post trigger information held in the store.

The trigger is still used to produce an analogue ramp; this is used by the sampling mode circuitry used to digitise repetitive waveforms on the top six ranges of the TIME/DIV switch, and it defines the rate at which data is loaded into the store. In ROLL and REFRESH the rate at which data is entered into the store is defined by a programmable digital divider which divides the master 20MHz clock under control of the TIME/DIV switch to provide 100 data samples per div unexpanded on the display. This is also the resolution obtained in the SAMPLING mode. Expansion of the display is carried out in the X amplifier by analogue means and this gives a resolution of 10 samples/div.

In digital storage mode only a line of alphanumerics is available which is produced under control of the microprocessor during the display period (see fig. 4). The microprocessor repeatedly monitors the positions of the two cursors and, when selected, displays both the time and voltage differences on this line of alphanumeric text.

4.2 THE Y AMPLIFIERS AND BEAM SWITCH

These circuits are shown in Fig. 7, Fig. 10.

The attenuators and pre-amplifiers of channel 1 are identical to those of channel 2 and accordingly only channel 1 is described.

The input signal is applied to SKA and then to the attenuator via the 3 position slide switch, S101. This allows the input signal to be directly coupled through in the DC position or coupled via C105 in the AC position. In the central GND position, the input signal from SKA is left open circuited while the input to the attenuator is grounded.

On the most sensitive ranges, 2mV/div to 100mV/div, the volts/div switch S101 couples the signal directly to the pre-amplifier, the input impedance being defined by R104. On the ranges 0.2V/div to 1V/div S102 introduces N102/5 and N102/6 into the signal path to provide an attenuation of 10:1. High frequency compensation of the attenuator on these ranges is provided by C109 and C104, while C102 allows the input capacitance to be set up to match that on the unattenuated ranges. On the ranges 2V/div S102 introduces N102/2 and N102/3 into the signal path to provide an attenuation of 100:1. High frequency compensation of the attenuator on these ranges is provided by C108 and C107 while C106 allows the input capacitance to be set up to match that of the unattenuated ranges.

Diodes, D201 and D202, with R207 provide input protection by limiting the input voltage applied to the amplifier to the voltages of zener diode, D203 and the positive supply line.

The input stage of the pre-amplifier is formed by the f.e.t. source followers, TR201 and TR202, and emitter followers, TR204 and TR203. Unbalance in this stage is corrected by the BAL control potentiometer, R301.

The input stage drives the divider network N201. The volts/div switch's second wafer S201 selects the necessary output either directly via RN201 on the 2mV range of attenuated by 2.5,10,25 or 50 times on the subsequent ranges as required. This network presents a constant output impedance and further attenuation is introduced by the shunt action of the variable sensitivity control R217. The resultant signal is amplified by the integrated circuit amplifier U301. The amplifier gain is determined by R309 and the preset R302. The differential output is balanced by the bias through R308 from the Preset R307.

The differential outputs from IC301 (CH1) and IC351 (CH2) are then split. High impedance amplifiers buffer the signals to the Analogue to Digital Converter (ADC) and convert the differential signals to single ended outputs (see Analogue to Digital Converter). The differential outputs also feed R316 and R317, which provide defined signal currents to the beamswitch, and these are summed with the Y shift currents defined by R318 and R319 from the CH1 shift control, R315. The corres-

ponding components for channel 2 are R366, R367, R368, R369 and R365. Channel 2 only differs for channel 1 by the addition of the double pole change-over switch, S301, which reverses the output signals from IC351 in the INVERT mode.

The signals currents from IC301, and IC351 are fed into a 3 way beamswitch with the stored signal from the Digital to Analogue Converter (DAC). The beamswitch is formed by diodes, D301, D302, D303, D304, D351, D352, D353, D354, D811, D812, D813, D814. In NORMal mode the output of inverter U826e is low, switching off Q806 and Q807, it also takes the junctions of D811 and D813 low, diverting the signal currents from R823 and R824 reverse biasing D812, D814. The junctions of D301, D302 and D351, D352 are then both under control of IC501b. The bistable controls the beamswitching of the two Y channels into the Y output amplifier (see 4.5 Mode Control Circuits). In STORE mode the output of the inverter U826e is high. This forces the junctions of D301, D302 and D351, D352 low via Q806, Q807, diverting the Y pre-amplifier signal from the Y output amplifier.

At the same time, the junction of D811, D813 is taken high, forward biasing D812 and D814 and allowing the signal from the Y DAC to drive the bases of TR401 and TR402 in the Y output amplifier. The outputs from the differential shunt feedback amplifier stage formed by TR401 and TR402, are fed to the grounded emitter amplifier stage, TR403, and TR404. This in turn feeds the differential cascode Y output stage TR405, TR406, TR407 and TR408 to drive the Y deflection plates of the c.r.t.

High frequency compensation of the output amplifier is provided by networks between the emitters of TR403 and TR404 and those of TR405 and TR406. Adjustment of this compensation is by C402 and C405.

4.3 TRIGGER CIRCUITS

These circuits are shown in Figs. 8 and 10.

The Trigger Source switches, S502 and S503, connect the required trigger signal via the Trigger Coupling switches. S504 and S505, to the trigger buffer amplifier formed by Q601 and Q602. S502 selects the differential CH1 signal via R313 and R315 from IC301 (Fig. 4). S503 selects the equivalent CH2 signal via R363 and R364 from IC351. Where both S502 and S503 are selected, both of the above signals are disconnected and the single-sided input from the EXT TRIG input socket SKC is selected.

When the AC coupling switch, S504, is out, the trigger signals are directly coupled-through, but when this switch is in, AC coupling is introduced via C603 and C604 (C601 on External). Q601 and Q602 form a differential buffer amplifier with the DC balance controlled by the TRIGGER LEVEL control, R602. The differential output from this stage is applied to the comparator, IC602, which has positive feedback applied by R623 to form a Schmitt trigger circuit. The change-over swhich, S506, reverses the output from Q601 and Q602 to determine the trigger slope.

When both S504 and S505 are "in" (AC and DC in for TV mode), the junction of R603 and C610 is connected to the –11V supply, D601 and D608 are brought into conduction while D602 and D604 are reverse biased. This diverts the output of the trigger amplifier away from IC602, into Q605, which amplifies the positive tips of the video waveform only. TR605 is prevented from saturation by feeding back the peak detected sync. pulses via Q607 and Q606 to the emitter of Q605. These pulses are amplified by IC601b and applied via R617 and D603 to the Schmitt trigger, IC602. IC601a is used in conjunction with S504 and S505 to disable the synch. separator when AC or DC is selected.

At the fast timebase sweep speeds, S262a is open and Q603 is cut off. However, at speeds of 100μs/cm and slower, R608 is connected to +11V and Q603 is switched on. This effectively grounds C609 to introduce an RC integrating time constant into the synch. pulse signal time path in the TV mode to separate out frame trigger.

The output of IC602 is used by the timebase generator (see next section).

4.4 ANALOGUE TIMEBASE GENERATOR AND X AMPLIFIER

The square wave trigger output from IC602 is applied (with d.c. bias of zener diode, D605) as the clock to the D type TTL flip-flop, IC501a. A positive-going trigger edge will clock the bistable driving $\overline{Q}$ low. In the waiting state. $\overline{Q}$ was high (+4.5V), turning on Q261 via R507 and R262, holding the input, and hence the output of the operational amplifier, IC261 at 0V. This timebase amplifier is connected as a direct voltage follower.

When the trigger signal sends $\overline{Q}$ of IC501a low, the timebase clamp transistor, Q261, is turned off. Part of the constant current generated by Q264 flows through the resistor network, RN272, to charge C263 at a constant rate. The resultant positive-going linear ramp voltage generated at the input of IC261 is buffered by that amplifier to generate the low impedance ramp output.

The timebase range switch, S262, selects the top point on the network, RN272, to vary the ramp store in the 1.2.5 sequence over a range of three decades. On all fast sweep ranges, Q262 is biased-off but on ramps 0.5ms/cm and slower, S262c connects R263 to +11V. Q262 is turned on and C264 is effectively connected in parallel with C263 to slow the sweep rate 1000 times.

The constant current into the ramp generator is derived from the current mirror circuit formed by Q263 and Q264. The variable gain control, R264 provides an approximate 3:1 range of variation in this current, R506 provides a preset calibration control on the slow sweep rates, only when S262c is closed.

When the ramp reaches its maximum level the negative bias, introduced by R521 and R519, is overcome and Q503 turns on, driving the reset input of the timebase bistable low. As the bistable switches, $\overline{Q}$ returns high and Q261 conducts to discharge the timing capacitor(s) and the sweep is complete. However, a hold-off action takes place to inhibit trigger signals during sweep and this remains for a short period after a sweep to ensure that the ramp potential is fully reset before the next sweep can be triggered. As the ramp goes positive, D506 conducts to charge C502, reverse biasing D503 and turning on Q502. At the end of the sweep when the timebase bistable is reset, $\overline{Q}$ goes low and the D input follows via the action of D508 and R511. The ramp output returns rapidly towards 0V but Q502 remains in conduction for a period determined by C502 and R518. Only when Q502 turns off can R516 and D507 take the D input high for the bistable to respond to the next clock input.

Q501 acts in a way similar to Q262 (described above) to introduce additional hold-off time through C501 on the slower half of the timebase ranges.

The AUTO facility causes the timebase to free-run in the absence of trigger signals. The square wave output from the Schmitt trigger, IC602, is coupled via C615 in to the peak detector diodes, D606 and D607, to generate a positive-going signal into the –ve input of IC601c driving its output negative. In the absence of such trigger signals for a period determined by C618 with R627 and R626, the output of IC601c goes positive. When Q502 turns off at the end of the hold-off period, D509 conducts to turn on Q504, driving the set input low to initiate another sweep.

This free-run condition is removed as soon as IC601c detects an output from the Schmitt trigger. When the o/p of IC601c is low it indicates the presence of a trigger signal. Q815 is then switched on, lighting Trigger l.e.d. D1.

This free-run condition can be inhibited by operation of the AUTO switch S501 which takes the junctions of D509 and D505 low via R562.

The output of the ramp generator IC261 is fed to the analogue multiplexer U821b. The other input of the multiplexer comes from the output of the Dot Joiner in the digital ramp generator (see digital ramp generator). In NORMal mode the ramp output from IC261 is selected by the output of U826e going low. The ramp is then buffered by U827, a unity gain buffer amplifier, which then drives the X output amplifier via R821 and C820. In STORE mode, the output of the digital ramp generator is selected and as in NORMal mode drives the X output amplifier via amplifier U827, R539, and C515.

The X output amplifier is formed by the shunt feedback stage of Q509/Q511 driving single sided into the amplifier stage, Q513 and Q514. The collector output of this stage drives the x deflection plates of the c.r.t. directly from Q514 and via emitter follower Q515 and Q513.

The gain introduced by Q509/Q511 is defined in the X10 magnification mode by the input resistance R539, and the feedback resistance, R552, with the preset, R553. In this mode the transistor switch, Q512, is biased off. However, in the normal X1 magnification mode S507 is open and the current in Q548 turns on Q512, introducing R544 with preset, R511, as additional feedback to reduce the gain of the amplifier accordingly.

The X shift control, R271, introduces an additional bias input via R541 and emitter follower Q506, through the potential divider R569/R545.

4.5 MODE CONTROL CIRCUITS

The display mode is controlled by S261 (Fig. 8) and the NORM/STORE button S1106.

S261 defines the state of three control lines, L1, L2, L3. The state of these control lines is then further defined by the gating U822a, f, d, e, U823a, b, c, d, U832a, b, c, U833a, d. The outputs of this gating DL1, DL2, DL3 are level shifted by Q808, Q809, Q810, and these outputs drive the mode control circuitry.

In NORMal mode, the state of DL1, DL2, DL3 follow L1, L2, L3 but in STORE mode these outputs do not follow L1, L2, and L3 (see table below).

Section 4.2 describes the action of beamswitching diodes, D301 to D304, D351 to D354 and D811 to D814, and as mentioned then in NORMal mode the diodes D301, D302 and D351, D352 are controlled by the outputs of beam switch bistable, IC501b. In the CH1 mode, DL1 is low allowing R525 to take the set input of the bistable low, Q is high and $\overline{Q}$ is low, selecting the channel 1 signal for Y display. In the CH2 and X-Y modes. DL1 is at +11V and R514 takes the set input high but L2 is open and R524 takes the reset input low to reverse the bistable and select the channel 2 signal.

In the Add mode, both DL1 and DL2 are low so that both set and reset are applied to the bistable, Q and $\overline{Q}$ are high and both channel signals are added into the shunt feedback stage of the Y amplifier (Fig. 4). In this mode only, DL1, DL2, and DL3 are open, removing the bias through D401, D402 or D403 and defined by R401 and R402 via D405 and D406. This offsets the additional bias introduced by the selection of both channel signals.

Only in the X-Y mode, DL3 is held at +11V to turn on the diode gate of D515 and D514, so coupling the channel 1 preamplifier signal of IC301, via Q506 and R547 into the X output amplifier. At the same time D504 conducts to turn off the gain switching transistor, Q512 thereby selecting x 10 X magnification irrespective of the positive of S507.

D501 conducts allowing current through R509 to turn on Q261, clamping the ramp generator so that no signal is fed into the X amplifier via R539. Finally, current through R512 turns on Q504, holding the timebase

NORMAL MODE

DISPLAY MODE S261	L1	L2	L3	DL1	DL2	DL3	IC501b Q	5
X-Y	+11V	0	+11V	+11V	0	+11V	L	H
CH1	0	+11V	0	0	+11V	0	H	L
DUAL	+11V	+11V	0	+11V	+11V	0	SWITCHING	
CH2	+11V	0	0	+11V	0	0	L	H
ADD	0	0	0	0	0	0	H	H

STORE MODE

DISPLAY MODE S261	L1	L2	L3	DL1	DL2	DL3	IC501b Q	Q
X-Y	+11V	0	+11V	+11V	0	0	L	H
CH1	0	+11V	0	+11V	0	0	L	H
DUAL	+11V	+11V	0	+11V	0	0	L	H
CH2	+11V	0	0	+11V	0	0	L	H
ADD	0	0	0	+11V	0	0	L	H

bistable set "on" to provide continuous bright-up of the trace,

In the Dual mode, both DL1 and DL2 are held at +11V so that the beam switch bistable, IC501b, is free of set or reset signals. Thus it can respond to clock signals and as its D input is connected to its Q output its state reverses on each clock input.

On the fast sweep ranges (0.2ms/div and above), the clock input is derived via emitter follower, Q505, directly from the Q output of the timebase bistable. Thus the beamswitch operates in the alternate mode. The Y deflection is switched between channels at the end of each sweep. Q506 and Q508 form a free-running emitter coupled multivibrator but on the above ranges, S262 f is open such that R534 is disconnected and the multivibrator is disabled.

On the slow ranges (0.5ms/div and below), R534 is connected to +11V and the multivibrator runs. During each sweep period, the multivibrator provides continuous clock inputs to the beam switch bistable so that the beam deflection signal is made to chop between the two channel signals. The beam switching is inhibited between sweeps as the emitter follower, Q505, clamps high the clock input to the beam switch bistable. In all modes but Dual, DL1 or DL2 are low and D512 or D513 conducts to inhibit the action of the multivibrator.

Ic601d is used for the 1kHz calibrator. It is connected as an oscillator with positive feedback via R629 and negative feedback via R633. This with C617 defines the frequency as approx. 1kHz. The output is buffered by the transistor switch, Q604, which defines the calibrator output amplitude via the potential divider of R638 and R643 with preset, R641.

In the STORE mode DL1, DL2, DL3, as shown in the table above, force all selections on S261 to be effectively CH2. The beamswitch bistable, IC501b then behaves as described above for this mode. However, since both outputs from the Y preamplifiers are disabled the beamswitch bistable does not control the input to the Y amplifier, and the Y amplifier is driven by the Y DAC.

4.6 THE ANALOGUE TO DIGITAL CONVERTER

These circuits are shown in Fig. 9, 10.

As described in Section 4.2 the differential CH1 and CH2 Y Preamplifier outputs are picked off and converted into a single output on the pick-off board.

The CH1 outputs of U301 are fed into a differential amplifier formed by Q1301, Q1302, whose gain is adjusted by R1329. On the normal DSO ranges, 50ms/div to 0.5ms/div Q1355 is turned on by the output of U805a. This output only goes high for timebase ranges of 20μs/div to 0.5μs/div. Q1355 when switched on connects C1351 across the roll off capacitor C1302, producing a high frequency roll off of approximately 1MHz.

A sample of the shift amount set by R315 is also differentially amplified by U1301a. The gain of this stage is adjusted by R1323 and the offset by R1325, adjustment of these two presets enables matching of the shift signals and the Y signals. The output of U1301a is added into the output of the differential amplifier Q1301 and Q1302. The resultant signal is buffered by emitter follower Q1304.

Transistors Q1305 and Q1356 together with associated components form a constant current source to the

collector loads of Q1302 and Q1352 thereby improving the power supply rejection ratio.

The circuitry of CH2 is identical to that for CH1. The circuit references for CH2 can be obtained by adding 50 to those of CH1, except for the CH1 components R1311, R1329, R1328, R1312, C1309, C1351, Q1355. The corresponding CH2 components for these are R1327, R1377, R1376, R1326, C1357, C1353 and Q1353.

The outputs of the emitter followers, Q1304 for CH1, Q1354 for CH2, drive a sample-and-hold.

The output Q1304 feeds the sample gate formed by D801, D802, D803 and D804. Normally the diodes, D803, D804 are held reverse biased by the zener diodes, D801 and D802. The control circuitry produces a 50ns sample pulse, when a conversion is required at the output of U803c. This pulse is amplified and converted into a differential signal by a long tail pairs, Q803 and Q804. The differential output of Q803, Q804 is applied to T801 pulsing the Shottky diodes D804 and D803 on for the duration of the sample pulse. These diodes conduct and allow C803 to follow the analogue input from Q1304. When the sampling pulse ends the capacitor holds the instantaneous value of the input. The diodes have a very low leakage and the hold capacitor C803 is buffered by a very high impedance amplifier formed by Q801a, b and Q802. The capacitor therefore has a low droop rate and the output of the amplifier will be held for long enough for the successive approximation converter (SAC) to convert the analogue signal accurately into a digital representation.

The sample-and-hold for CH2 behaves in exactly the same way as outlined above for CH1, with all circuit references being 9XX instead of 8XX (except U803).

The two sample-and-holds hold the value of analogue signal at the sampling instant and their outputs are beamswitched by the switch formed by Q805 and Q905. The beamswitch is controlled by the Q $\overline{Q}$ outputs of the bistable Q935a. The Q high, Q805 is switched off and D909 is reverse biased. Hence Q905 is conducting and the output of the CH2 sample-and-hold is presented to the input of the SAC. With the Q output low the CH1 output is routed to the Successive Approximation Register. The D input to the bistable is the CH1 signal from U831. (see Section 4.7 for details of timings). This is clocked by the Start Convert signal from U803b, delayed by U801a, b by approximately 10ns, which initiates the conversion cycle of the SAC U815. The SAC has a 20MHz Xtal oscillator to control its internal logic. This is formed by U801f, U801e, C847, R867, R868 and XL801. The output of this oscillator is gated by U805b, so that the clock can be disabled externally and by the NORM/STORE button, thus reducing the amount of breakthrough in NORMal mode. If the 20MHz clock is disabled and external clock can be used via U802a.

The SAC conversion cycle is initiated as stated above by Start Convert. The conversion takes 9 20MHz clock cycles, i.e. 450ns, and it takes approximately 50ns for Start Convert to initiate the conversion. The complete conversion cycle takes 500ns. At the end of the conversion cycle the digital word representing the analogue input is latched onto the D0-D7 outputs. The SAC will nominally produce a code of 00000000 for an analogue input of 0V and 11111111 for -0.5V the reference level input. However to compensate for the variation in gain of the pick-off buffer amplifier and sample-and-hold, the reference input to the SAC can be adjusted by R842 to -0.5V ±0.1V. This ensures that a CH1 or CH2 input signal that should cause a full screen deflection produces a range of codes from the ADC of 00000000 to 11111111.

4.7 TIMING AND CONTROL LOGIC

The timing signals used by the SAC are produced by the relatively high speed logic circuits around U807, a four bit decade counter. This counter is clocked by the 20MHz clock. Outputs QA QB and QC which is inverted by U829d feed gate U805c which resets the bistable U806b on a count of three. This reset takes the Q output high. When the count reaches eight, QD goes high, clocking the bistable U806b, taking $\overline{Q}$ output low. Thus the WE input to U831 is high from a count of three to eight, which is a period of time fo 250ns.

A counter output of eight is detected by U804a, the output of which goes low. On the next ninth clock this low is clocked through bistable U806a producing a positive going edge on the Q output. On the tenth clock the Q output remains low. This output therefore is a 50ns pulse that occurs on a count of nine of the counter U807. This pulse passes through two inverting gates U802c, U803b and is further delayed by U801a and U801b. This pulse clocks bistable U835d and also initiates a conversion cycle of the S.A.C.

The 50nS pulse at a 2MHz repetition rate, produced by U804a, is inverted by U809d and applied to U831 pin 54.

The LD input on Pin 9 of U807 is driven by U804c. One input of this gate will be high when RESET STORED and/or STORED (PIN 3 U831) are low. The other input of this gate will be high when RESCH1 (Pin 51 U831) is high. RESCH1 is driven high by U935b which is clocked by EWRITE (Pin 50 U831). The reset input of this bistable is determined by the microprocessor, depending on the setting of the Time/Div switch. A five bit code is derived from this switch, from a wafer mounted on the switch pick-off board (see Fig. 16). This code is read by the microprocessor via U913 which in turn generates a 4 bit code, through U911 pins 5,2,9 and 6. This four bit code D1,D2DIV2 and DIV5 is shown in Table 1.

The output of gate U805a is high for all but the top six ranges when an all ones code is detected. This output is inverted by U826c. The output of this inverter is the

TABLE 1 ULA TIMEBASE CODES

RANGE/DIV	TB4	TB3	TB2	TB1	TB0	DIV2	DIV5	D1	D2
0.2s	0	0	0	0	0	0	0	0	0
0.1s	0	0	0	0	1	0	0	0	0
50ms	0	0	0	1	0	1	0	0	0
20ms	0	0	1	0	0	0	1	0	0
10ms	0	1	0	0	0	0	0	1	0
5ms	1	0	0	0	1	1	0	1	0
2ms	0	0	0	1	1	0	1	1	0
1ms	0	0	1	1	0	0	0	0	1
0.5ms	0	1	1	0	1	1	0	0	1
0.2ms	1	1	0	1	1	0	1	0	1
0.1ms	1	0	1	1	1	0	0	1	1
0.05ms	0	1	1	1	0	1	0	1	1
20μs	1	1	1	0	1	1	1	1	1
10μs	1	1	0	1	0	1	1	1	1
5μs	1	0	1	0	0	1	1	1	1
2μs	0	1	0	0	1	1	1	1	1
1μs	1	0	0	1	0	1	1	1	1
0.5μs	0	0	1	0	1	1	1	1	1

1 is TTL HIGH
0 is TTL LOW

SAMPLE signal. When SAMPLE is low, this takes the output of U809b high and hence the reset input of U935b low forcing RESCH1 high.

SAMPLE controls the selector formed by U802b, U802c and U803d. When SAMPLE is low, the Q output of U806a is routed through to the SAMPLE AND HOLDS, via U802c and U803b. U806a hence controls the sampling of the input signals, the sample pulse being the same width and timing of the clock to the beam-switch bistable U935a described earlier in this section. When SAMPLE is high the sample pulse is derived from the outputs of U904a. Again the pulse is approximately 50ns wide but its occurrence is controlled by the sampling circuitry described later (Section 4.11).

The waveforms described above are shown in Fig. 3.

4.8 STORE CONTROL AND INTERFACE CIRCUITRY

The data from the ADC, or processed display data from the microprocessor, is stored in a 2048*8 static RAM (U919). There are two signals controlling the writing of data into this store. The first of these is R/W signal (U1447/8) which is under control of the microprocessor board and is discussed in section 4.15. The second is the NMWE signal which is used for the normal writing of the ADC data into the store.

The timing signals controlling the writing of data into this store are produced by U831, an uncommitted logic array (U.L.A.). This U.L.A. produces a Read/Write control signal $\overline{\text{NMWE}}$ (see Fig. 4 for timing). This signal consists of double pulses, each 250ns in length at a rate determined by the TIME/DIV switch and by the Sampling Pulse produced by U904a (see Section 4.11 for descriptions of relevant circuitry). This signal $\overline{\text{NMWE}}$ latches the data from the ADC into a TRISTATE buffer U816 and controls the $\overline{\text{Output Enable}}$ line of this buffer. When $\overline{\text{NMWE}}$ goes low the data held in this latch appears on the outputs Q_0 to Q_7. Simultaneously the output buffers of the memory are put into a high impedance state by this signal eliminating contention on the data bus. Meanwhile U831 has produced a write address on lines A0 to A9 (U831 PINS 39, 38, 37, 36, 35, 34, 32, 31, 30, 29). These address lines are buffered by U924 and U926 before being applied to the store. The output enable signal for these two buffers is MEME controlled by the microprocessor board. For the first of the two negative going pulses of $\overline{\text{NMWE}}$ A10 (U831 PIN 28) is low and when $\overline{\text{NMWE}}$ goes high again the data held in the buffer is stored in the address selected by A0-A9 and A10. When $\overline{\text{NMWE}}$ goes low a second time, the new data from the ADC is latched into the buffer and again the stores' data lines go to high impedance. The lines A0-A9 still contain the same write address but A10 now has

gone high so the new data is stored into the upper half of the store. When $\overline{\text{NMWE}}$ remains high in this way CH1 and CH2 data is stored at a rate selected by the NMWE signal into their respective halves of the store.

When $\overline{\text{NMWE}}$ goes high the second time, the stores internal memory buffers are enabled and the stores will contain data from the address selected by A0-A10. Within the U.L.A. the write address is incremented after the second write. Reading of this data is again controlled by the U.L.A. U831. On all ranges below 0.2ms/div reads are interleaved with writes of a 200kHz rate. Thus the address lines A0-A9 contain alternatively a write 'slot' and a read 'slot', each 'slot' lasting 2.5μs, enabling continuous reading and writing to occur. For the three ranges above 0.5ms/cm the store is completely filled with data, during which the display is blanked, writing is then prevented and the data is then displayed. This process, under control of the microprocessor, then repeats so that a complete write followed by a read occurs continuously. However if in single shot mode acquisition occurs only once followed by the normal read out cycle which continues indefinitely.

The read and writes are interleaved continuously at 200kHz rate so that for each new read 'slot' there is a new read address. This address is presented to the store which then places on its data lines the data contained at this address. At the end of the read slot RWCLK goes low, latching the Read Data into latch. The output of this latch drives the DIGITAL TO ANALOGUE CONVERTER (see section 4.9). Note that in Roll mode, for ranges of the TIME/DIV below 0.2ms/div the read address will increment by two if a write has occurred in the previous write slot. This causes the continuous 'rolling' effect visible on the display in this mode.

The waveforms associated with the store control circuitry described above are shown in Fig. 5.

Once a 'read' of the lower 1024 addresses of the store is complete, A10 goes high for the next 1024 'read' slots so that the upper half of the store is read.

The writing to and reading from the two halves of store are controlled by the DISPLAY MODE switch, S261. The three signal lines L1, L2, L3 derived from this switch are decoded and level shifted by gates, U822a, d, f, b, and U823b, c, d. (see table in Section 4. for L1, L2, L3 codes). This gating produces two signals NCH1, and NCH2, NCH1 is low if X-Y or CH1 is selected and NCH2 is low if CH2 or ADD is selected on the MODE switch. If both lines are high, Dual channel operation is selected. The operation of the Dual Channel mode has been described earlier in this section.

If however either NCH1, or NCH2 is low the U.L.A. U831, forces line A10 to the memory low for NCH1 low and high for NCH2 low. Thus writing and reading of only the relevant half of the store occurs. One of the NMWE double pulses is also inhibited if either CH1 or CH2 is low, 'NCH1 low' inhibiting the first of the two pulses enabling only relevant information from the A.D.C. to be latched into the store and its latch. The beamswitch bistable is also controlled by NCH1, and NCH2. If NCH1 goes low, the bistable is RESET and the beamswitch forced over to CH1, and vice versa if NCH2 goes low.

The process of converting and storing data has been described above. However, the selection of when a write cycle should occur and the associated operating mode are controlled by ARM RELEASE, 25% and 75% PRETRIGGER, HOLD ALL, HOLD CHANNEL TWO, ROLL/REFRESH, ARM AND RELEASE control whether the data is captured in a single shot mode or in a continuous mode. The ARM button S1101 initiates a single shot acquisition of data. The arm button S1101 is monitored by the microprocessor via U912/17 and when activated causes the micro to initiate an arm signal from U911/16. This ARM signal takes low the reset input of the bistable U814/C producing a low on the output Q. Hysteresis on the reset input is provided by resistors R892 and R893. The bistable output is inverted by U826d and the resultant high level triggers one half of a dual monostable U1101, via input 2B, and allows timer U1102 to oscillate at a period of 2Hz. This is set by R1107, R1108, C1104, and provided ARMLED ENABLE is high, the l.e.d. D1101 will flash at this rate. ARMLED ENABLE is controlled by the microprocessor via U911/12 and is normally high on all ranges except the three ranges above 0.5ms/cm. On these ranges this signal is taken low when in released mode so that the l.e.d. does not flash persistently. The time constant of this half of dual monostable, U1101, is set by C1102 and R1105 to be 100μs, and so on triggering, the Q output of this monostable will go low for 100μs. This negative going 100μs pulse arms the ULA U831. If the STORED output of this device was high, it will now go low. If REFRESH is selected by pushing in the ROLL/REFRESH button, the address lines of the U.L.A., during the write slots as described earlier in this section, remain at zero, until a trigger occurs. TRIGGER signals are disabled initially on ARM by latch, U839a. The latch is held set by S1101 and the $\overline{\text{Q}}$ output is low, disabling U812a and preventing triggers passing through this gate. When S1101 is released, the set input of U838a goes high after the length of the time constant set by C854 and R872. When the TRIG input next goes low it resets U838a taking the $\overline{\text{Q}}$ output high, enabling gate U812a and allowing triggers to reach U813b. When not in SAMPLING mode, the output of U805a is high, taking PIN1 of U813b high and PIN 11 low. The output of U812a will then be inverted by U813b and triggers the U.L.A. when the TRIG input goes high. The output of U813b also drives U812b. The other input of this gate is high, again since $\overline{\text{RELEASE}}$ is high, taking low the output of U826f and forcing the output of U812c high. The inverted TRIG signal will thus take low the SET input of bistable U814c, forcing high the Q output, and low the output of U826d. This will take high the RESET on timer U1102 resetting the output, and switching off Q1101. The l.e.d. D1101 will extinguish.

Once the U.L.A. has received a trigger signal, the write addresses will increment from zero, at a rate determined by the TIME/DIV switch, and at each successive store location, data from the ADC will be stored, as described earlier. When all 1024 store locations in each half or in one half of the store have been updated, the stored output of U831 will go high, taking low the output of U804b, high the output of U809a, and low the output of U829e. The STORED LED D1101 on the functions switch board will now light indicating that acquisition of data has now ceased and the display is now stored.

The operation of ARM in the ROLL mode is essentially as described above except that the write addresses begin incrementing immediately after the ARM to U831, and the ULA U831 ignores TRIG signals. When a sufficient amount of data has been entered into the store to satisfy the pretrigger requirements, the U.L.A. will now accept a TRIG signal. When the required amount of post trigger information has been stored, writing will cease and the STORED output of the U.L.A. will go high, as in REFRESH. As data is written into the store the read address increments so that an increasing offset occurs between the Read Address to the STORE and the address lines to the DAC, U931, causing a 'rolling' effect on the display. The display ceases rolling when the STORED indication occurs, since writing ceases.

When ARM is operated, it also clocks bistable, U836a. The D input of this bistable is driven by gate, U824a. If the TIME/DIV switch is selecting ranges 0.05ms/div, 0.1ms/div and 0.2ms/div, the output of either U833b or U833c will be low, taking high the output of U824a. If ROLL mode is selected the output of U824c will be low, again forcing high the output of U824a. The output of U824a therefore indicates that either one of the three timebase ranges mentioned above, or ROLL mode has been selected by S1105. Therefore the Q output of bistable U836a will be low if ARM is operated and the output of U824a is high, forcing high the output of U824b, selecting ROLL mode to the U.L.A. until RELEASE or RESET or hold goes low, when the output of U824b will follow the state of the ROLL/REFRESH signal from S1105.

Operation of the release button triggers the monostable on the function switch board. The monostable has a time constant of 47ms set by R1104 and C1101 and will thus produce a negative going 47ms pulse. This pulse is monitored by the microprocessor via U912/6 and is actioned from U911/16 clearing the stored condition and resetting U836A which enables the ROLL/REFRESH signal to the ULA to follow the ROLL/REFRESH button. In refresh, the operation of RELEASE essentially enables continuous recycling of the write cycle described above for ARM. The write address holds at zero until a trigger occurs, at which point, the write address begins incrementing, data being stored in each successive location. When the STORE has been filled with new data, writing ceases until another trigger is received when the writing process begins again.

This cycle repeats indefinitely until the operating mode is altered.

In ROLL after operation of the RELEASE button, the write addresses to the store begin incrementing immediately, new data being stored at each location in succession. Again as in the ARMed mode the read address to the store increments by one extra count after each write, causing the rolling effect on the display. The write process occurs continuously and is unaffected by the TRIGGER signal, and the display as a result will roll continuously, new data appearing on the right-hand end of the screen and rolling across the screen to the left-hand side.

On the top three ranges of the TIME/DIV switch for which ROLL and REFRESH are applicable, 0.2ms/div, 0.1ms/div and 0.05ms/div, the display is blanked while data is being acquired and then after acquisition is complete the new data is displayed. The rolling effect on both ARM and RELEASE is therefore not present on these ranges. However data is required in exactly the same fashion as described above.

The amount of pretrigger information stored in ROLL mode is controlled by the two buttons 25%, 75% PRETRIGGER. When both buttons, S1103 and S1104, are out the signals PER 25 and PER 75 are both low, and with either S1103 or S1104 operated the relevant signals PER 25 or PER 75 will go high to indicate 25% or 75% PRETRIGGER has been selected. With both switches operated both signals will go high indicating 100% PRETRIGGER selected. These two control signals PER 25 and PER 75 are used by the U.L.A. U831, to control the acquisition of data with respect to the trigger point. If REFRESH mode is selected control signals PER 25 and PER 75 will both be low, indicating 0% PRETRIGGER, regardless of the state of the two PRETRIGGER buttons, S1105 forcing a low output from both S1103 and S1104.

Operation of Display hold freezes the display, holding the information present on the screen. When the DISPLAY HOLD button, S1404 is out, the set input of bistable U814c is high, and the reset input is low. This forces output Q low which is monitored by the microprocessor through U912/13. The hold output from the processor is through U933/7, forcing the output of U826B high. The D input of U836b is thus high and so when DAC10 of U831 goes high, halfway through a read cycle the Q output will be clocked high, producing a low of the output of U824d, and taking N HOLD on U831 and one input of U809c high. The U.L.A. U831 will take a high level as indicating a NOT HOLD signal. The $\overline{\text{NMWE}}$ signals will reach the memory enabling data to be written to the STORE as described earlier.

If the display HOLD is operated i.e. pushed in, the set input of U814c will go low and the Reset input will now be high taking the Q output high. This is detected by the processor through U912/13 which responds by taking the D input to U836b low by asserting a high

output on U933/7. When DAC10 next goes high during a read cycle the low on the D input to U836b will be clocked through to the Q output. This produces, a positive clock edge at U836a, latching either the state of the ROLL/REFRESH, or a logic high if the TIME/CM switch is on the ranges 0.2ms/div, 0.1ms/div and 0.05ms/div, as described earlier. The N HOLD input of U931 is taken low, freezing the write address produced by the U.L.A. for the memory, preventing further locations in the store being updated. Gate U809c is also disabled driving high $\overline{\text{NMWE}}$, and hence preventing data being altered at the current write address.

When CH2 hold is operated this is detected by the microprocessor via U912/11 as an active low signal. The processor responds by taking U933/10 high, which in turn taked U905/13 high. A positive going A10 signal at U924/2 will now take U905c/10 low. This stops the second of the two NMWE pulses from passing through to U905b thereby preventing the updating of information in the CH2 part of memory.

4.9 DIGITAL TO ANALOGUE CONVERTER

Digital Y data can come from either the display store or the microprocessor and the data is then applied to the D/A converter U820. The normal store data is latched into U918 by the RWCLK. The output enable for this device is controlled by the DACE line from the microprocessor board. The inverse of this signal also controls the output enable of U917, another latch, which is connected to the microprocessor's external data bus. Hence only one of these two latches can be enabled at a time.

The Y data present on the output of latches U917 and U918 is converted into an analogue form by U820, a monolithic eight bit digital to analogue converter. A reference current is fed into this device and the Io and $\overline{\text{Io}}$ outputs produce a differential current output proportional to the produce of this reference current and the digital code present on its data inputs Do to D7. Resistors, R886 and R887, set a reference current of 1mA, giving Io and $\overline{\text{Io}}$ a range of 0 $\longrightarrow$ 1mA depending on the digital code selected. The reference current is derived from a 6V2 voltage reference formed by Zener Diode D910 and R944 decoupled by C943. Approximately one quarter of the Io and $\overline{\text{Io}}$ currents are fed into the differential amplifiers, U827a and U827d, which convert the currents into a voltage output of approx. +280mV.

A time constant of 1μs, set by C822 R830 and R831, is applied to this differential output. This matches the time constant of the digital ramp generator, and provides a dot joining effect on the display, the dot moving linearly between the data points, through the brightness increases non-linearly as the dot moves between the data points. An adjustment of the relative d.c. offset of the differential Y output signals is provided by R829 enabling the two Y output signals to be balanced. The outputs of this amplifier is fed into Y beamswitch via R823, R824, R371, R372 as described in section 4.2.

4.10 DIGITAL RAMP GENERATOR

The U.L.A. provides a linearly incrementing address bus DAC1 to DAC10 to drive a 10 bit digital to analogue converter (DAC). The lines DAC1 to DAC10 increment from 0 to 1024 as the Y data is read out of the store, 0 corresponding to the left-hand edge of the screen, and 1024 the right-hand edge of the display. These ten address lines DAC1 to DAC10 are first buffered by U929 and U930 before being applied to U931, a monolithic 10 bit DAC. The output enable's for these two buffers are connected to the DACE signal, signal which is controlled by the microprocessor board. The DAC inputs are also connected to the X ADDRESS BUS from the microprocessor board. This produces the differential current outputs Io and $\overline{\text{Io}}$ which represents the product of the digital word on the data inputs and the reference current into the device. The reference current is set a 1mA by R845 and R846 which are connected to 0V(A) and the 6V2 voltage reference mentioned in the previous section.

The current $\overline{\text{Io}}$ which flows to U931 pin 2 derives from R844, the difference current feeding into R847. The voltage of 0 to +1V generated across R847 is buffered by the unity gain buffer, U825b (see Plot section 4.12).

The Io current output of U931 pin 4 is fed to amplifier, U825a, which converts it to a voltage output. The gain of this amplifier is set by preset, R834. A time constant of 1μs on the output is set by R833, R822 and C821 to match the time constant in the Y D.A.C. output amplifier (a small analogue ramp is added into the amplifier input in sampling if necessary. See 4.11) The output of the D.A.C. has a glitch at the changeover of the m.s.b. To reduce this a sample of the m.s.b. is fed into the inverting input of the output amplifier via R849 and C830. The output of the amplifier drives one input of the multiplexer U821b via R833. The other input of this multiplexer is the analogue ramp output from IC261. When NORMal is selected the analogue ramp is fed through to the X output amplifier, and in STORE mode the digital ramp is fed to the X output amplifier, U826e controlling the multiplexer.

The U.L.A. U831 produces a digital blanking signal which lasts for the first four counts of the count on lines DAC1 to DAC10, i.e. 20μs wide. This digital blanking signal is lengthened to 30 micro seconds wide by R946, R949, D911 and U906b. The extended blanking signal is monitored by the microprocessor through U929/12 as is the state of the NORM/DSO line. The output enable for this half of the buffer is also controlled by the microprocessor board. The blanking signal is then OR'ed with a blank signal from the CPU by U906a before being multiplexed with the anlogue blanking signal from the

collector of Q507. In NORMal mode, the analogue blanking signal is selected and in STORE mode the digital blanking signal is selected, the selected signal driving the Bright-up amplifier described in section 4.16, which provides blanking of the display when the c.r.t. beam flies back from the right hand side of the screen to the left hand side and also provides blanking for the alphanumerics as required.

4.11 SAMPLING

These circuits are shown in Figs. 10.

On the top six ranges, 20μs/div to 0.5μs/div, a repetitive sampling method is used to obtain a digital representation of the input waveform.

This technique uses the analogue ramp described in Section 4 and the digital ramp generator formed by U831 and U931 described in Section 4.10.

The aim of this technique is to obtain 1024 samples of the waveform in the time, selected by the TIME/DIV switch necessary to sweep 10.24div across the screen. In the following discussion a TIME/DIV selection of 1μs/div will be used to illustrate this technique. The time taken to sweep 10.24div is, using this figure of 1μs/div, 10.24μs. if we need 1024 samples of the waveform in this time, the samples must be taken at intervals of 10ns. Now the analogue timebase ramp must have the necessary slope to sweep the beam across 10.24div of display in 10.24μs. If the amplitude of the ramp required to produce 10.24div of deflection is A Volts, this slope is A/10240 V/ns. Therefore if the samples are taken at intervals of 10ns, this corresponds to a voltage interval of $\frac{A}{10,240} \times 10$, or $\frac{A}{1024}$ Volts

The slow ramp level in fact must increment at A/1024 Volt intervals to produce 10.24div of display at full scale. Hence a comparator driven by the fast analogue ramp, (which starts at a defined point on the input waveform) and the output of the digital ramp, will produce pulses every time the fast ramp crosses the slow ramp. If the slow ramp after every crossing, increments by one level, i.e. A/1024V, the crossing point will increment at intervals of 10ns. If a sample of the input waveform is taken at each crossing the required objective of taking a sample at 10ns intervals from the trigger point is achieved, each successive sample occurring on successive fast ramps. The ciruitry necessary to implement the above method will now be described in detail.

The sampling process is initiated by operating the ARM button. This takes low the reset on U814C, producing a high on the output of U826d. This will enable U812d, allowing the TRIG signals from IC501a pin 5 in the analogue timebase circuitry to clock counter U902. This TRIG signal goes high at the beginning of fast ramp and low during the fast ramp holdoff. Since U812d inverts the TRIG signal the counter is clocked at the end of the fast ramp.

To ensure that the slow ramp starts above the fast ramp, and hence ensure that the comparator will produce a positive going output, a Start-up circuit is incorporated which offsets the slow ramp until a crossing is obtained.

When the instrument is armed, the Q output of bistable, U904a, is low, and bistable U904b is reset. Counter U902 is then enabled by the Q output of U904b so that the counter will increment at the end of each fast ramp.

R921, R922, R923, R924, R925, R926 on the outputs of this counter produce a current into R836 on the non inverting input of amplifier, U825a, proportional to the count on the counter. Therefore as the counter increments, the output of U825a will be offset in a positive direction. The output of U931 is, at this time, constant and the data input from DAC1 to DAC10 is zero. The line DAC1 to DAC10 are incremented by the TRIG signal to the U.L.A. U831 which, at this time, are disabled at gate U813b pin 9, by the output of U904b.

When the output of amplifier, U825, is offset sufficiently so that the non inverting input of comparator, U903, is at a higher level than the lowest point of the fast analogue ramp, which is fed into the inverting input of this comparator from the output of IC61, the comparator will produce a positive going edge at its output. This output is fed back into the non-inverting input via R919 to ensure a sufficient amount of hysteresis at the switching point, preventing oscillation at this point. This positive-going output clocks a 'high' through bistable, U904a. The D input of this bistable has a time constant ensuring that for a short time after an ARM, the D input remains low, so that comparator crossings are ignored until the D.A.C., U931 has settled. The Q output of the bistable, U904a, will go high, once the comparator has produced a positive edge, and the D input has gone high. The Q output of U904a remains high for approx. 50ns after the Q output has gone high, producing a 50ns pulse at the output of U804d. As described in section 4.6, this pulse drives the sample and holds at the inputs to the SAC beamswitch.

The Q output of U904a going high clocks bistable U904b, producing a high on the Q output, and a low on the Q output.

The enable to counter, U902 goes low, the counter stops incrementing, holding a fixed offset on the output of U825a U831 pin 47. Note that the TRIG input of U813 pin 10 has a time constant formed by C853 and R871. This ensures that the positive going output of U813b is delayed by approximately 2μs after the fast ramp finishes. This positive going output causes the D.A.C. outputs of U831 to increment, thus increasing the level of the slow ramp at U903 pin 2. When that fast ramp rises again, the comparator produces another positive going edge, delayed by one sample interval from the previous edge. Meanwhile when the fast ramp reset, and TRIG went low, bistable U904a was reset, and so this edge from the comparator will clock U904a and so produce another sample pulse. This sequence of events

will repeat until 1024 sample pulses have been produced and the output of D.A.C. U931 has reached its maximum value. At this point the STORED output of U831 will go high. This produces a low at the input U808c setting flip-flop, U814c, disabling the clock input to counter, U902, taking low the D input of U904a and resetting U904b. The output of U809a will also go high, resetting counter, U902 and driving low the output of U829e which switches on the STORED L.E.D. D1101. the U.L.A. U831, outputs (DAC1 to DAC10) now increment at the read rate as described section 4.10.

The 1024 negative-going sample pulses which are produced by U804d during the sampling process, not only drive the sample-and-holds in the A.D.C. but also initiate a conversion and store cycle for each sample taken that initiates conversion of the samples and then ensures the data produced by the A.D.C. is stored correctly.

In the Sampling mode, the output of U805a is low, taking high the output of U826c, this being the SAMPLE signal. $\overline{\text{SAMPLE}}$, the reverse of this signal, is produced by U826a. U804d produces the 50ns sample pulses. When SAMPLE is high, these pulses are gated through U801c, U803d and U803c to the sample-and-hold circuitry (described in Section 4.6). These pulses are inverted by U809b which is enabled in SAMPLE, and again inverted by U829c, and resets bistable, U835b, taking low the Q output. The Q output was previously high, and so the $\overline{\text{LD}}$ input of counter U807 was low, presetting the counter outputs to 7, the value determined by the A,B,C,D, preset inputs. The Q outputs of U835b going low clears the LD input on U807, and so on the next 20MHz clock, the counter will increment to a count of eight. Referring to Fig. 5, the counter and associated circuits will produce a WE signal at the Q output of U806b, a MHZCLK to U831 pin 54 and a Start convert signal to the SAC U815, as described in Section 4.7.

The timing logic will produce four start convert pulses, four write enables and four MHZCLK signals, at which point a positive edge is produced by U831 pin 50, clocking bistable U835b so that the Q output returns high, setting the LD input of U807, which presets the counter to a count of 7 and holds the count until LD returns high.

As the timing logic produced these pulses, U831 produces an A10 signal to determine which half of the store is to be written, an address on lines A0 to A9 to determine which location is to be written and a $\overline{\text{NMWE}}$ signal which writes the data into the store. A10 is clocked low by the first of the MHZCLK input to U831, and alternates after each MHZCLK ending high after the fourth MHZCLK signal. Address lines A0-A9 remain constant for the whole of this cycle and increments only when the TRIG input to U831 goes high, at the end of each analogue ramp, $\overline{\text{NMWE}}$ is delayed and inverted version of the WE input to U831, hence four of these signals occurs, each going low 50ns approximately after A10 changes, latching the address on the store address bus into the store. When $\overline{\text{NMWE}}$ returns high 250ns later, the data at the store data bus is latched into the store. The data latch U816, latches data from S.A.C. U815, and enables its output buffers when NMWE goes low, so that the memory receives new data from the A.D.C.

4.12 PLOT

A plot facility is fitted as standard on this instrument. The option of either a digital plot or analogue plot is selected by switch SW1 which is read via U1440 on the microprocessor board. The digital plot is carried out under software control and is discussed in section 3.7.7.2. The analogue plot is initiated by operation of either the PLOT1 or PLOT2 buttons and provides an output suitable for either an X-Y or T-Y pen recorder.

Operation of the PLOT1 button takes the set input of bistable U814a low and the reset input high forcing the Q input high. When the button is released the Q output is forced low. The output Q is monitored by the microprocessor via U912/2 (U912/14 for PLOT2) which responds by taking U933/2 high, provided switch SW1 is set for analogue plot. The output of U933 initiates the plot mode for CH1 via the PLOT1 input of the ULA U831. The PLOT output of U831 will go high, thus switching the analogue multiplexer U821a so that the output of U821b is routed through to the X ramp output, and after the first four Y data samples have been read out enables the output of U827c to pass through multiplexer, U821c, to the plot Y output. The plot signal is inverted by U829A which drives into the A input of monostable U828A. The B input driven by the TSTMON output of U831 is already high, and the monostable fires, driving high the Q output, and low the $\overline{\text{Q}}$ output for approx. 500ms, the period set by R851 and C838. The CEP input of counter, U807, is taken low and so the counter halts, holding up the plot operation 500ms. The set input of bistable, U838b, is driven low for 500ms, taking high the Q output, and taking low the penlift via open collector gate U832d. After 500ms plot continues and the data is readout from the store and reconstructed by DAC U820. The current output of U820 is converted into a bipolar voltage output by amplifier U827c, at approx. an output level of 100mV/div.

The X ramp output is produced by D.A.C. U931, in synchronism with Y data readout. One of the current outputs of this D.A.C. drives amplifier, U825b, which converts this current into unipolar, voltage output at a level of approximately 100mV/div. When the data has been plotted TSTMON pin 18 of U831, having been low during the plotting, returns high. The A input of U828

This cycle repeats for each of the 1024 sample pulses, with A0 to A9 incrementing after each cycle when TRIG goes high. After a full store of data is acquired, the STORED signal from U831 goes high, as described earlier, ending the data acquisition. Reading of this data will now continue until another single shot capture is requested via the ARM button.

is still low at this time and so U828 is retriggered, again halting counter, U807, for 500ms, holding the Plot outputs at the last point plotted. The reset input of U838 will also go low for 500ms, taking high the penlift output, U832d. After 500ms the plot mode will be disabled and the display will return to the normal readout rate.

Operation of PLOT 2 is the same as PLOT 1, bistable U814d being replaced by U814a in the above description.

4.13 CURSOR AND SWITCH PICK-OFF BOARDS

The cursor switch board (see Fig. 15) is used to mount the cursor control buttons below the CRT on the front of the instrument. When operated each switch (S1–S5) connects its control line to ground pulling low one of the inputs to the microprocessors I/O port. Each line has a pull up resistor on the CPU board. Capacitors C1-C5 remove spurious noise spikes from these control lines.

The switch pick-off board (see Fig. 16) is mounted behind the Pre-amp board and holds three switch wafers which are used to generate codes for the microprocessor. One of these codes is the timebase code discussed in section 4.7. The other two switch wafers generate a code (see Table 2) depending on the setting of the input attenuators, one wafer being used for each channel. These codes are accessed by the microprocessor via latch U914 on the interface circuit. Pull up resistors for all three switch wafers are also mounted on the interface circuit. Capacitors C1702-C1713 remove spurious noise spikes from the switch lines.

TABLE 2. Attenuator Codes

RANGE	INPUT CODE				HEX
VOLTS/DIV	Y3	Y2	Y1	Y0	
10	0	0	0	0	0
5	1	0	0	0	8
2	1	1	0	0	C
1	0	1	1	0	6
0.5	1	0	1	1	B
0.2	0	1	0	1	5
0.1	1	0	1	0	A
50mV	1	1	0	1	D
20mV	1	1	1	0	E
10mV	0	1	1	1	7
5mV	0	0	1	1	3
2mV	0	0	0	1	1

4.14 RS423 CIRCUITS

The majority of the serial transmission circuitry is contained in the microprocessor itself. All data and control lines are accessed via PORT2 of the micro. Transmitted data from U1401/12 is first inverted by U1434 before being sent to the RS423 board (see Fig. 17) through PL1601. The data for transmission as well as the REQUEST TO SEND (RTS) line are converted to RS423 standard by U1601, an RS423 driver device. Wave shaping is carried out by C1601 and C1602. Received data and the CLEAR TO SEND (CTS) signal, if applicable, are converted from RS423 standard to a unipolar voltage by the receiver device U1602. All the necessary lines for the RS423 interface are accessed through a 25 way D-type connector on the rear of the instrument.

4.15 C.P.U. BOARD

The CPU Board is based around a 6303A, a 1.5MHz CMOS mircoprocessor operating in its multiplexed mode. The memory map for this particular system is shown in Table 3 and the circuit diagram for the CPU board is shown in Fig. 18. Components C1401, C1402 and XL1401 set the frequency of operation of the CPU at 1.2MHz.

POWER ON RESET

When the 6303 microprocessor is powered-up the mode of operation is determined by the logic levels on Port 2 PINS 8, 9, 10. As mentioned earlier the mode of operation in this case is the multiplexed mode and this is selected by holding PINS 8 and 9 low and PIN 10 high during power-up. Components R1401 and C103 apply the reset signal to U1401 and at the same time provides the correct logic levels to the CPU via U1404. The time constant of the RC combination is approx. 100ms. After this period the RESET input to the CPU and U1404 goes high allowing the Port 2 lines to be used for I/O. The threshold of U1401/6 is set lower than that of U1404 so that reset is completed before U1404 changes state.

MEMORY DECODING

The components used in the memory decoding are U1420, U1421, U1422 and U1448d. U1422b decodes the memory map into four 16K blocks. The two top 16K blocks are used for the EPROM IC's U1407 and U1408 (optional). The section from 16K to 32K is used for the I/O registers and alphanumerics RAM. This 16K Block is split into 2K sections by U1420 and U1421. These two IC's are enabled by the R/W line and the E clock in such a way that U1420 decodes the Read only Ports and U1421, the write only Ports. The lower 16K portion of memory is split into 4K Blocks. The top two 4K segments are combined by U1448d and are used for the RAM. The next 4K Block is used for the display RAM U919 on the Interface/DSO circuit. The lowest 4K Block is left uncoded and is used by the microprocessor itself for its I/O Ports and Timer etc.

DSO INTERFACE

This circuit is formed by U928, U927, U923 and U925 on the interface circuit and U1418, U1419, U1431, U1432, U1433a,c,e,f, U1434a,b,f, U1435a,c, U1436, U1437d, U1439a,c,d, U1446, U1447 and U1448b on the CPU Board. (See Fig. 13 and Fig. 14).

The function of the interface circuitry is to provide the CPU with access to the Display RAM U919 and the I/O Ports mounted on the DSO circuit without affecting the normal display sequence. When the I/O Ports are addressed U1446 pin 1 is set high, this connects the B inputs to the Y outputs of U1446. U1418 and U1419 are now held in their transparent state. When a read port is addressed U1447b goes low enabling the output of U1419. This creates a path from the input Port through U1419 to the microprocessor. When a write port is addressed U1437d goes low enabling the output of U1418. This creates a path from the microprocessor through U1418 to the output Port via the external data bus.

If the instrument has at any time since power-up been in ROLL mode then the data corresponding to the left hand edge of the CRT display has no set address within the display strore. Hence for the microprocessor to access the Display RAM it is necessary for it to know how the left hand edge of the screen relates to the Display RAM address.

The signal RTC is a 5 microseconds pulse which goes low when the right hand edge of the display is reached. This signal after being inverted by U1433c and gated with the R/W CLK (U1447a) is used to latch the address on U927 and U928 on the interface circuit. This terminal count address is then used by the microprocessor to calculate physical addresses within the display RAM.

When the display RAM is addressed U1446 PIN 1 is set low connecting the A inputs of U1446 to the Y outputs. For a write operation U1431/9 is also set low. DATA is then written to the correct Display RAM address by latching the address in U923 and U925 and then writing the DATA through the external data bus. If the operation is a READ then the address is latched in the same way and the data is read through U919.

For a write Data is stored in U1418 and the lowest eleven address lines are held in U923 and U925 on the interface circuit. The microprocessor sets U1431/16 high clearing the reset on U1432. This enables RWCLK to be shifted through U1432 at a rate of 0.5 micro-seconds per stage. The gating around U1432 combines these shifted outputs to give the signals detailed in the timing diagram Fig. 5A. The R/W signal U1447 pin 8 only goes low during write cycles. Normally this signal is high and hence DIR, U1447d/11, is also high. This signal controls U916 on the interface circuit. The output enable of this device is the RAMSEL line generated from the shifted inputs of U1432. For a read operation DATA is stored in U1419 which the microprocessor can get by reading any valid DISPLAY RAM address.

ALPHANUMERICS AND CURSOR GENERATION

The following elements are used for the generation of the alphanumerics and cursors: U1430, U1431, U1433b,c, U1435d, U1437b and c, U1438, U1440a and b, U1441, U1442, U1443, U1444, U1445. An internal functional diagram of the PAL U1438 is shown in Fig. 5C and a timing diagram of its function is shown in Fig. 5B.

Every 15ms, unless in RSS or Sampling, the PAL initiates an alpha cycle by stealing one of the ULA display cycles. Exactly 5ms is allowed for the display of the alphanumerics and cursors before the PAL relinquishes control to the ULA.

In RSS, data is acquired and then the display is blanked. After acquisition cycle stealing is carried out after two cycles on ranges 0.2ms/cm, 0.1ms/cm and after four cycles on 0.05ms/cm. In sampling mode the display is again blanked during acquisition, and then after acquisition then the display starts with a cycle being stolen for alphanumerics every 15ms.

At the beginning of an alpha cycle NMI is taken low causing an interrupt request in the microprocessor. The display dot is positioned one quarter of the way across the screen in X and just above the base line in Y. This drives the output of U1435d high enabling U1442 and U1443 to count. These two IC's are clocked by E/4 which is gated in the PAL such that the clock is only enabled during the alpha period. The E/4 signal is derived by dividing down the E clock through U1445a and U1445b. When a count of 192 is reached U1435d goes low again disabling further counting. These outputs form the 8 most significant bits of the X-DAC and cause a half screen line to be drawn. The alpha RAM U1444 is also addressed by these 8 lines and its output forms the blanking signal which is superimposed onto the alphablank line. the microprocessor detects when U1435d goes low and then draws another line in the same manner but slightly lower. Seven lines in total are drawn, giving 16 characters on a 7 x 8 grid. At the end of the seventh line U1431 pin 5 goes low which disables the clock to U1442 and U1443. These devices now behave as latches. The microprocessor draws the cursor as a series of dots by directly controlling the X and Y DACS. The X Data is placed on the address bus (10 bits) and the Y Data on the Data Bus. The X DAC latch is formed by U1441, U1442 and U1443 with the Buffer formed by U1430 and U1440. The Y DAC latch U917 is on the interface circuit.

INPUT/OUTPUT PORTS

Throughout the interface and CPU Board there are 8 input Ports and 6 output Ports. (The tables show in details which control lines are present at each Ports (See Tables 4, 5). Read Output Ports and Write Output Ports are denoted by either ROP or WOP as necessary. ROP01 monitors the cursor control buttons while ROP02 is used for the RS423 interface and the mode select lines on power up. ROP03 monitors keypad data (optional) and the state of the two control lines DSO/NORM and ULABLNK. ROP04 is used to monitor the ongoing status of the interface board. ROP05 and ROP05L hold the RTC address that is latched at the end of a display. ROP06 and ROP07 monitor the timebase and channel attenuator input codes respectively.

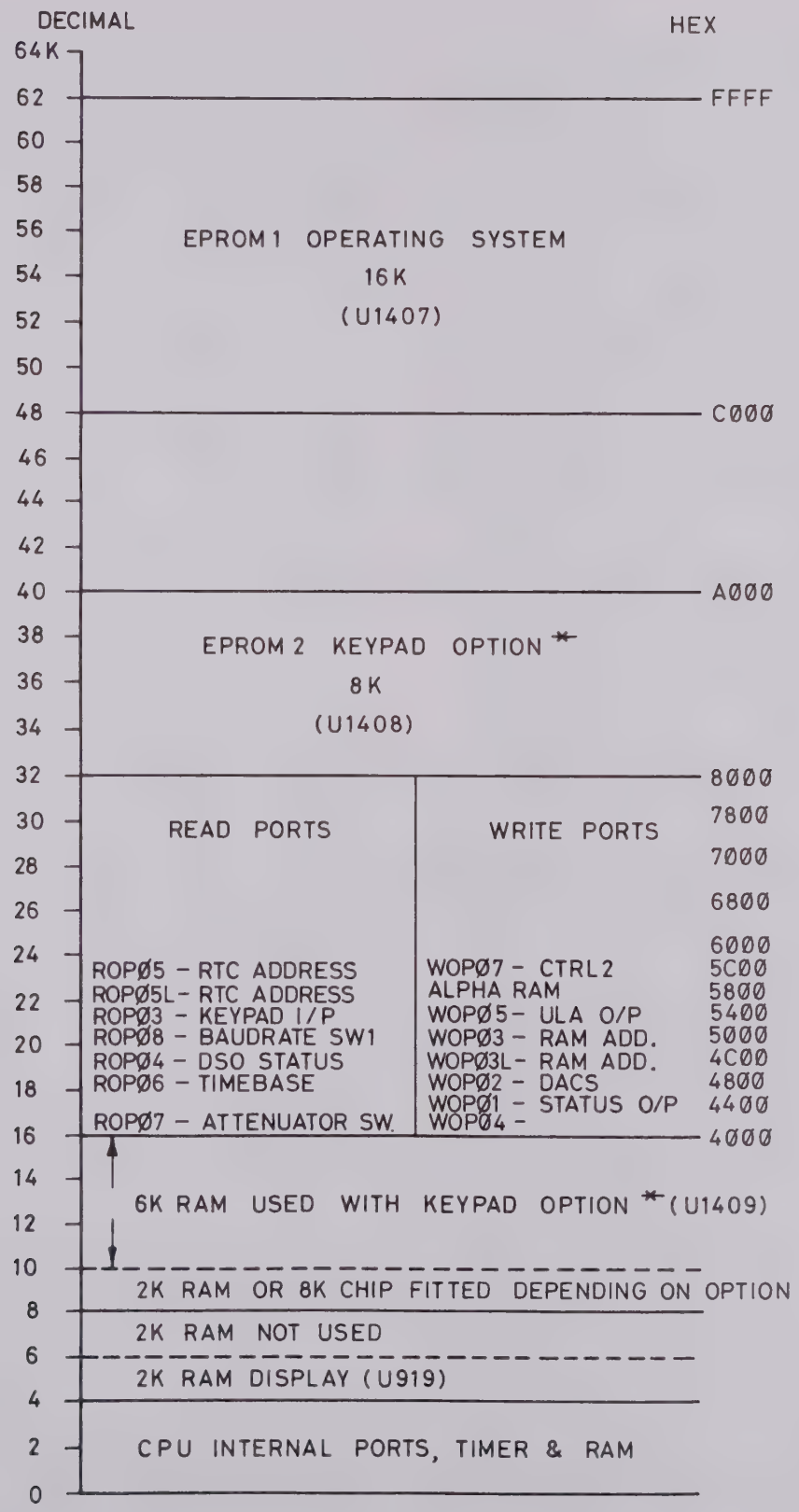


Table 3 Memory Map

TABLE 4
READ PORTS

PORT	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ROP1	ON/OFF	SET DATUM	CH1/ CH2	SHIFT RIGHT	SHIFT LEFT	NCH2	NCH1	END OF LINE	0002
ROP2	–	–	–	TX	RX	P22	P21/CTS	P20/RTS	0003
ROP3	ULA BLANK	DSO/ NORM	DB5	DB4	DB3	DB2	DB1	DB0	5400
ROP4	ARM INPUT	STORED	HOLD ALL	HALF HOLD	DIV1K	RELEASE INPUT	PLOT2	PLOT1	4000
ROP5	–	–	–	–	–	MA10	MA9	MA8	5000
ROP5L	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	5800
ROP6	–	–	X10	TB4	TB3	TB2	TB1	TB0	4800
ROP7	Y23	Y22	Y21	Y20	Y13	Y12	Y11	Y10	4000
ROP8	–	–	–	–	SW1D	SW1C	SW1B	SW1A	5000

TABLE 5
WRITE PORTS

PORTS	D1	D6	D5	D4	D3	D2	D1	D0	HEX
WOP1	FAST DISPLAY	START TRANSFER	ALPHA ENABLE	MICRO BLNK.	TRANSP. MODE	MODE	NMI BLNK.	DUAL	4400
WOP2	D7	D6	D5	D4	D3	D2	D1	D0	4800
WOP3	–	–	–	–	–	A10	A9	A8	5000
WOP3L	A7	A6	A5	A4	A3	A2	A1	A0	4000
WOP5	N/C	RELEASE OUTPUT	ARM OUTPUT	ARMLED ENABLE	DIV2	DIV5	D1	D2	5400
ALFRAM	–	–	–	–	–	–	–	D0	5800
WOP7	–	–	–	–	HALF HOLD O/P	HOLD ALL O/P	PLOT2 OUTPUT	PLOT1 OUTPUT	5000 5000

ROP08 is used to monitor the state of the switch SW1 and is discussed under OPERATION section 3. The output port WOP01 is used to control the reading and writing of data to the interface board and the alpha-numeric circuitry. Data written to the Y DAC from the CPU is done so through WOP02. WOP03 and WOP03L are used to hold the RAM address when the CPU writes to the display RAM. WOP05 and WOP07 are used when writing or echoing control signals monitored via ROP04. The alpharam is written too using the least significant bit of the data bus through ALPHRAM.

4.16 POWER SUPPLIES AND C.R.T. CIRCUITS

Circuits for the power supplies are shown in Figs. 11, 12.

The following D.C. supplies are generated in the power supply circuits from secondary windings on the supply transformer, T.1.

+210V, +11V, +12V, +7V ,+5V, -5V, 11V, -1850V.

The +210V line is used primarily in the X and Y output amplifiers. The -1850V line is the cathode supply for the c.r.t. An additional 5V line is generated in the timebase from the +11V line by IC552 (Fig. 8).

The incoming a.c. supply from the supply connector, PLM, is switched by S1 and fuse protected by FS1 before reaching the two supply range switches, S2 and S3. S2 connects the two primary windings of T1 in series or in parallel for 120V or 240V operation while S3 selects the necessary tap for 100V or 220V operation.

The output from the 210V secondary is bridge rectified by the four bridge-connected diodes, D722 to D725, into the reservoir capacitor, C705. The resultant d.c. voltage protected by FS701 feeds the h.t. regulator for the +210V supply. D730 is the reference for this supply, buffered by emitter follower, Q711, and the Darlington pair, Q713. The return of the rectified 210V supply is via the 11V line to balance load current in the low voltage supplies.

The four low supplies +11V, +7V, -5V (used on the main p.c.b. assembly), and -11V are derived from a single 25V secondary of transformer, T1. Its output is bridge-rectified by bridge connected diodes, D726 to D729, into the reservoir capacitor, C704.

The distribution with respect to the 0V line of the voltage across this capacitor is determined by the -11V shunt regulator and the +11V series regulator. The -11V reference is provided by the Zener diode, D711, with temperature compensation diodes, D713 and D714 and. Q720, while shunt transistor, Q712, conducts to maintain the -11V line at the correct potential.

The -5V line is derived from this -11V line by the zener diode, D712, with the compensation diode, D720, followed by the emitter follower, Q709.

With the negative side of the unstabilised supply across C704 defined at -11V by that stabiliser, the positive side is applied to the series regulator, IC702, which takes up all variation in the unstabilised supply to define the +11V line. This is a 15V regulator with 'low' pin 3, returned to a -4V potential defined from the -5V supply by R735 and R734.

The +7V supply is provided from the +11V supply by a further 12V series regulator, IC701, operating with respect to the -5V line.

All the above outputs are connected to the subsequent oscilloscope circuitry via split pads in the copper track pattern. These are normally bidged by solder but can be used to isolate each line to assist fault finding.

Other supplies of +12V,5V and -5V are generated on the auxiliary power supply board (see Fig. 12) as is a line trigger output of about 1 volt. The line output signal is derived from a winding on the secondary of T1 and is filtered by components R1201 and C1210 before being fed to the line output socket on the rear of the instrument.

The +12V, +5V and -5V supplies are derived from secondary winding on T1 of 14V, 8.5V and 8.5V respectively. The 14V output is bridge-rectified by D1205, D1206, D1207 and D1208 and smoothed by C1204 and C1205. A 12V regulator U1202 provides a regulated supply of 12V, which is decoupled by C1206. The +5V and -5V supplies are produced in a similar manner, the relevant components being D1201, D1202, D1203, D1204, C1201, C1202, U1201, C1203 and D1209, D1210, D1211, D1212, C1207, C1208, U1203 and C1209.

The grid and cathode supplies for the c.r.t. are derived via the voltage doubler circuit D718, D719, C711 and C712, from the 950V secondary of T1. The negative side of the unstabilised supply developed across C711 and C712 is held at approx. -200V with respect of 0V by the series zener diode, D706, which is returned to the stabilised cathode potential of -1850V. Subsequent variations in the unstabilised supply are developed across the series regulator, Q707, of the e.h.t. regulator. The feedback path of this regulator uses the current from the -1850V line defined by the resistors R715, R714 in parallel with R744 (the Focus pot.) and RN720e. The latter being within the e.h.t. network. This current is returned to the +7V line via R731, R725 and R726. If the resultant potential of the tap point defined by the preset, R725, is not at approx. -4.5V, the current in transistor, Q706 will change to correct the stabilising voltage across Q707, Q706 and Q707 are connected in cascode.

The heater of the c.r.t. is supplied directly from an independent 6.3V secondary winding of T1.

The 1425 employs a novel modulation circuit to control the grid potential with respect to the cathode potential. The transistor pair, Q703 and Q704, generate an essentially constant current from the collector of Q703. This generates a constant voltage across RN720 and preset,

R713 and is returned to ground via the output of the bright-up amplifier. Thus signal variations from this amplifier which operates with respect to 0V are transferred with the large negative d.c. offset to the collector of Q703, to be applied to the grid of the c.r.t. via the emitter follower Q716.

In more detail, the constant current from Q703 is defined by the emitter resistance, RN720c and the base potential, from the divider, RN720a and RN720b.

This constant current source is returned to the -200V line (negative of D706) so that the collector of Q703 (the c.r.t. grid) can move negative from the cathode. The collector potential is protected by D705 against excessive swing during switch-on or switch-off conditions. While RN720d and R713 generate the necessary large d.c. potential to couple the bright-up signals to the grid, the high frequency components are by-passed through C702.

The bright-up signal amplifier is formed by the cascode transistor pair, Q701 and Q702, with shunt feedback via R704. It responds to the sum of five inputs. The first is a d.c. bias via R707 from the INTENSITY control, R745. The second is the external Z Modulation signal from SKG, via R703. The third and fourth are the signals from the blanking selector. U813a, which in NORMAL provides bright-up during each timebase sweep with blanking of each chop transistion if appropriate, and in STORE mode provides bright-up on each readout sweep. Diodes D701 and D702, provide protection against excessive external inputs and with R702, prevent saturation of Q702.

The fifth input (P34) is derived from the microprocessor board and is used to balance the intensities of the alpha-numeric display and the normal readout display.

The focus electrode of the c.r.t. is supplies from the focus control potentiometer, R744, with a portion of the -1850V supply. The astig. electrode is supplied from preset, R708 driven from the +210V supply via the divider network R746, R747.

Minor angular misalignment of the gun assembly of the c.r.t. or the effects of externally applied magnetic fields, axial to the c.r.t., can be corrected by the trace rotation coil. This coil is round the neck of the c.r.t. and the current is determined by the TRACE ROTATION control, R737, connected between the ±11V supplies and driving emitter followers, Q714 and Q715.

5.1 GENERAL

Fig. 2a, 2b and 2c show the internal location of the major components, subassemblies and preset controls. No regular maintenance is required apart from the routine recalibration. The construction of the instrument is such that full access to all calibration controls and to most components can be obtained once the two halves of the case have been removed (See section 5.2).

Supply voltage adjustment is made by the two selector switches on the rear panel. The supply fuse is mounted adjacent to these switches and the supply connector. This connector should be removed or the instrument switched off before operating the switches. For 100 or 120V operation a 800mA, 20mm slo-blo fuse is required (Part No. 454897), for 200 to 240V operation a 400mA 20mm slo-blo fuse is required (Part No. 454896). Disregard Fuse rating quoted on rear panel on early sets.

5.2 REMOVAL OF THE CASE AND SUB-ASSEMBLIES

WARNING

DANGEROUS VOLTAGES ARE EXPOSED ONCE THE CASE IS REMOVED. MAINTENANCE SHOULD BE CARRIED OUT ONLY BY QUALIFIED PERSONNEL. PARTICULAR CARE SHOULD BE TAKEN ON THE C.R.T. AND THE E.H.T. AREA OF THE MAIN PRINTED BOARD WHERE VOLTAGES IN EXCESS OF 2000V ARE PRESENT. THESE VOLTAGES MAY BE RETAINED AS STORED CHARGE FOR UP TO ONE MINUTE AFTER THE SUPPLY IS DISCONNECTED.

(a) To remove the Case (Top section)
DISCONNECT FROM THE SUPPLY.
Remove the two fixing screws at the top front sides and lift the top cover up and forward to clear the front moulded frame and the rear plastic moulded cover.

(b) To remove the Case (Lower section) and Handle assembly.
DISCONNECT FROM THE SUPPLY.
Remove the two fixing screws at the top front sides and proceed to remove the top cover as detailed in (a) above. Rest the instrument upside down and remove the screw from the centre of the front frame, securing the cover. Holding the lower case by the handle, pull both sides of the handle away from the case (as when adjusting the handle), then lift it up and forward so that the handle insert clears the side panel on the right and the strut on the left. The case can then be eased from the rear plastic moulding, holding the front of it clear of the front moulding. It may assist this operation if the screws holding the rear moulding are slackened but not removed.

(c) Removal of the C.R.T.
Remove the case as described in (a) and (b) above. Disconnect the trace rotation coil leads from pins 734 and 735 on the main printed circuit board. Unplug the tube base assembly. The base itself is carried on a small printed board which has been designed to allow access to facilitate withdrawal from the c.r.t. pins. Remove the single clamp fixing screw (see Fig. 2) and rotate the two clamp sections approximately 30° to free the clip from the centre panel. Once the tube and clamp assembly are free the clamp itself can be slackened on the tube. Slide the tube backward through the centre panel until the c.r.t. face plate is clear of the front mounting clip. The tube can then be lifted up and drawn forward, to clear the top edge of the front panel and frame moulding of the instrument. Withdraw the tube from the shield and the two part clamp.

When fitting a new tube, operate in the reverse order to the above instructions, with the exception of the tube clamp and centre panel fixing screw. On re-assembly the fixed part (rear) of the c.r.t. clamp is located in the slotted locating holes in the bulkhead and the retaining screw is fitted. The tube is then held forward against the graticule in the front moulding whilst the clamping ring is rotated to hole and lock the tube in place. Do not over tighten this ring.

Check the polarity of re-connection of trace rotation coil leads. Clockwise rotation of the front panel preset control should cause a corresponding movement of the trace.

(d) Removal of the DSO and Analogue pickoff board.
In order to gain access to the switch pickoff board and the front end assembly (attenuators and preamp), the DSO board and analogue pickoff board assembly will need to be removed as follows.

First remove all plugs and sockets from the DSO board, then remove the nuts holding it to the transformer and back panel. Swing the board up on its hinge to about 60° from the horizontal, then remove socket PLEE from the analogue pickoff board (mounted underneath the DSO board) and the trigger coax socket from the DSO board. Lower the board onto the transformer again and remove the nuts holding the hinge bar. The DSO and analogue pick boards should then lift off as one assembly.

(e) Removal of the Switch pickoff board.
Unplug PLXX and PLUU from the DSO board and unsolder the earth wire from PLUU to the attenuator screen. Remove DSO board fixing screws and socket PLEE and the coax socket as described in (d), then swing the DSO board assembly right over the front end allowing access to the switch pickoff board. This is supported by two pillars from the pre-amp board, on the side near the c.r.t., and two shafts through the switch wafer on the opposite

side. Remove the circlips securing the wafer to the switch shafts and slide the board off the two pillars and switch shafts, taking care not to damage the wiring under this board. Once the board is clear of the attenuator switch shafts it can be lifted clear.

NOTE: Ensure that the attenuator and timebase wafers (on switch pickoff board) and switches (on front panel) are set to the same setting as when the assembly was removed, before reassembling.

(f) Removal of the Attenuator assembly.
If access to the Preamp board, or the front of the main analogue board or the attenuators themselves is required, then proceed as follows.

Remove the DSO and Analogue pickoff board assembly and the switch pickoff board as described in (d) and (e). Remove the collet fitted knob on the timebase switch. Access to the collet securing screw or nut is by prising off the clip in the centre cap on the knob. Remove the small push on knobs on the two Variable Sensitivity controls, the Mode switch, the Trigger level, the Variable Sweep and X Shift controls. Remove the screen covering the preamplifier assembly, by unsoldering the three securing points on the front and the two on the back, unclipping it and sliding off the attenuator switch wafer shafts. Unsolder the three earth wires (coming from the main analogue board) from the 3 vertical screens, and also the screens themselves from the points where they are soldered to the pre-amplifier board. Unscrew the nut holding the solder tag attached to braid connected to the side screen, from the front of the main analogue board heatsink/support.

Unsolder and remove the wires from the CAL 1V pin and the EXT trigger connection on the input printed circuit board. Unsolder also the two signal pre-amplifier board.

The sub section front panel, carrying with it the two attenuator volts/cm switches, the two AC/GND/DC switches and the input coupling printed circuit board can now be un-latched by springing the four latch fingers away from the moulded frame and withdrawing the complete unit.

Re-assembly is the reverse of the aforementioned.

NOTE: Ensure that the attenuator and timebase switches are set to the same setting as when the assembly was removed, before reassembling.

(g) Removal of Cursor Switch board.
Remove the collet fitted knobs on the Focus and Intensity controls. Access to the collet securing screw is by prising off the clip in the centre cap of the knob. Unplug PL4 from the CPU board then unscrew the two nuts in the plastic moulding directly above the Cursor switch board (assuming the set is upside down). It can now be withdrawn from the plastic moulding though the potentiometers will still be connected to the wiring loom.

(h) Removal of the Input Coupling Switch printed circuit assembly.
If it is necessary to gain access to the small printed board which carried the input selection switches and the A.C. coupling capacitors for each Y channel, together with the input network for the External trigger signal proceed as follows. Using a desoldering tool, unsolder the tags of the input screen, clear the holes of solder and remove the screen. Unsolder and remove the two wires connecting the input printed board with the two attenuator wafer sections of each volts/cm switch. Desolder the three input B.N.C. sockets from this board and the three screen earthing points. The board should then be free for removal by easing upward, off the screen tags, then rotated to enable the switch sliders to clear the front moulding, and so withdrawn.

Re-assembly is the reverse of this sequence.

5.3 FAULT FINDING

Before any fault location is attempted, it is suggested that all supply voltages are checked. Subsequent signal voltages and waveforms should then be checked according to the following list which may be used as a general guide and aid to servicing. Note that the three typical voltages for unstabilised supplies are quoted for nominal mid-range supply voltages.

If a fault cannot be cleared it is recommended that the instrument is returned to the manufacturer for repair (see section 7).

When faults have been cleared it is recommended that the setting-up procedure of section 5.4 is followed.

For checking the supply lines there is a row of test pins, separated by bridge split pads. These pins will give outputs of +11V, −11V, +210V, +7V and −5V and if required the currents drawn by each line can quickly be measured simply by breaking the solder shorting the split pad for normal working operation, and inserting a current measuring meter between the two pins. In all five cases the line feed is nearer to the rear of the instrument, whilst the line load is connected to the forward pin.

The +12V +5V, −5V supplies for the DSO board may be monitored on the D.S.O. board at PLZZ. The fault finding tables define a suggested procedure to localise the fault to one particular area. Subsequent detailed guidance will be obtained from the relevant circuit diagram and circuit description and from the table of operating potentials.

Normal Operating Conditions
Unless otherwise specified the controls are set for single channel operation with the trace centred and timebase running. Potentials are specified with respect to ground and should be measured with a high impedance voltmeter, digital voltmeter or oscilloscope as appropriate. The NORMal switch should be set to NORMal unless otherwise specified.

(a) Supplies Unregulated

30V DC across C704 from 24 r.m.s. secondary voltage

268V DC across C705 from 210 r.m.s. secondary voltage

2.5kV DC across C711 + C712 from 950V r.m.s. secondary voltage

12V DC across C1201 from 8.5V r.m.s. secondary voltage

20V DC across C1204 from 14V r.m.s. secondary voltage

12V DC across C1207 from 8.5V r.m.s. secondary voltage

Stabilised		
+210V	± 21V	
+11V	± 0.5V	
+7V	± 0.4V - 0.6V	
-5V	- 10.4V - 0.6V	
-11V	± 0.5V	
+12V	± 0.6V	From auxiliary supply board
+5V	± 0.25V	From auxiliary supply board
-5V	± 0.25V	From auxiliary supply board

(b) Y-amplifier

Test Point	D.C. Level	Sensitivity
TR203/204 Collector	+7V	-
IC301, pin 1	+1V ±0.8V	-
IC301, pin 14	+1V ±0.8V	2mV/div
IC301, pins 7, 8	+3.5V	65mV/div each side
U827a	+3.9V	70mV/div With NORM /STORE
U827d	+3.9V	70mV/div switch in STORE

Test Point	D.C. Level	Sensitivity
Q401/402 Collector	+3.7V	40mV/div each side
Q403/404 Collector	+7.7V	140mV/div each side
Q405/406 Collector	+12.6V	-
Q4057/408 Base	+15.6V	-
Q407/408 Collector	+115V	6.8mV/div each side

(c) Analogue Ramp Generator

Test Point	Signal
Across R265 or R266	0.8V d.c. at "cal" 0.3V d.c. at min.
IC261 pin 3 and pin 6	+3.7V ramp from 0.1V level
Q264 Collector	+3.7V ramp from base level between 0 and +4V dependent on sweep rate selected.

(d) X-amplifier

Test Point	D.C. Level	Signal
Q512 Collector	+0.65V (Centre Screen)	500mV/div 6.0V ramp
Q511 Emitter	+3.7V (Centre Screen)	500mV/div 6.0V ramp
Q514 Base	-3.0V	-
Q513/513	+118V	12V/div each side 140V ramp each side

(e) Trigger Amplifier

Test Point	D.C. Level	Signal
Q601/602 Base	0V on Ext. 0V on Int A.C.	65mV/div each side
	+3.5V on Int D.C.	65mV/div each side
Q601/602 Collector	-4.8V	25mV/div each side

On TV mode:- Q601 and Q602 collector drops to between -8.5V and -10.5V dependent on the setting of the Trig. Level Control.

IC602, pin 9. Trigger output switches between -2V and -5.6V levels.

(f) Timebase Control

Test Point	Signal
IC501, pin 14	+5V, ±0.25V
IC501, pin 1	+5V (+1V at end of ramp)
IC501, pin 2	+4V (0V during hold-off)
IC501, pin 3	Trigger pulses between -0.5V and +2.8V levels
IC501, pin 4	+5V (0V during reset by bright-line)

Test Point	Signal
IC501, pin 5	+0.2V between sweeps +4.5V during sweeps
IC501, pin 6	+4.5V between sweeps +0.2V during sweeps
IC501, pins 8, 9	Beam switched between +0.2V and +4.3V levels

IC501, pins 10, 13	−0.6V or 4.5V depending on mode switch setting.
IC501, pin 11	Chop/alt. pulses between +0.2V and +4.7V levels
IC601, pin 8	+0.5V triggered or bright-line off +0V bright-line operating
IC601, pin 9	0V triggered or bright-line off +9.5V bright-line operating

(g) Bright-Up Amplifier

Test Point	Signal
Q507 Collector	Switching signal +4.8V (Blank) to 0V (Bright-up)
U831 pin 52	Switching signal +5.0V to 0V (STORE selected on NORM/STORE switch)
Q702 Base	+2V
Collector	Between +6V and +48V dependent on intensity
RN720, pin 4	−2kV
RN720, pin 5	+50V with respect to pin 4
RN720, pin 6	+340V with respect to −1850V

(h) Analogue to Digital Converter

For following measurements set instruments into STORE mode at 0.5ms/div.

Test Point	D.C. Level	Sensitivity
Q1302 Collector		65mV/div
Q1304 Emitter	0V	65mV/div
U1301a pin 1		65mV/div
D804, D803 Junction	0V	65mV/div
Q802 Emitter	−0.25V	65mV/div
Q805, Q905 Base		
U815 Pin 16	−0.25V	65mV/div
Pin 2	50ns pulse 0	4V signal
Pin 18	20MHz Clk. Switching 0	4V

(i) Control and Timing Logic

Instrument in STORE mode at 0.5ms/div

Test Point	Signal (TTL Levels 1 = TTL high Level 0 = TTL low level)
U807 pin 8	1
U804a pin 3	50ns Negative-going pulse
U805c pin 8	50ns Negative-going pulse
U806a pin 6	50ns Positive-going pulse
U801e pin 10	20MHz Clock
U802a pin 3	20MHz Clock
U8066 pin 8	2MHz Clock with even mark/space
U803c pin 8	50ns Positive-going pulse
U807 pin 11	100ns Positive-going pulse
U807 pin 7	1

(j) Store Control

Instrument in STORE mode at 0.5ms/div

Test Point	Signal (TTL logic levels 1 = TTL high level 0 = TTL low level)
U831 pin 46	1
U831 pin 48	200 kHz clock even mark/space
U831 pin 27	Two 250ns Negative-going pulses every 5μs
U831 pin 47	1 during ramp 0 during hold-off
U831 pin 52	20μs positive-going pulse every 5ms
U831 pin 18	5μs negative-going pulse every 5ms
U817 pin 21 U816 pin 1	Same as U831 pin 27
U816 pin 11	2 250ns positive-going pulse every 5μs

(k) Digital to Analogue Converter

Instrument in STORE mode at 0.5ms/div

Test Point	Signal (TTL logic levels unless otherwise specified)
U834 pin 11	200kHz clock
U819 pin 11	200kHz clock
U820 pin 13	+6.2V
U827a pin 1	3.9V D.C. level Sensitivity 70mV/div
U827d pin 14	3.9V D.C. level Sensitivity 70mV/div

(l) Digital Ramp Generator – X ∝-numeric Signal

Test Point	Signal
U831 pin 23	200Hz clock with even mark/space
U825a pin 1	200Hz ramp from 0V to 3.5V + alpha numeric signal (see Fig. 5D)
U821 pin 4	200Hz ramp from 0V to 3.5V + alpha numeric signal (see Fig. 5D)

(m) Sampling Circuitry

Instrument in STORE mode at 20μs/div

Test Point	Signal
U903 pin 1	2.5V analogue ramp at sweep rate selected on TIME/DIV switch
U903 pin 2	2.5 digital ramp at 200Hz rate
U903 pin 4	0 to 4V when slow ramp crosses fast ramp

U804d pin 11	50ns pulses at Trigger rate, when updating the Store, after ARM, before STORED indication lights.

(n) CPU Board

During power up.

Test point	Signal
U1401 pin 6	0V slow ramp to +5V
U1401 pin 8	CMOS low
U1401 pin 8	CMOS low } With U1401 pin 6 <0.7V
U1401 pin 8	CMOS low

After power up.

Instrument in stored mode, 0.5ms/div.

U1401 pin 40	1.228MHz CMOS 1:1 M/S
U1401 pin 39	1.228MHz CMOS 1:3 M/S
U1401 pin 4	5ms TTL low, 10ms TTL high
U1401 pin 5	5μs negative going pulse every 5ms
U1445 pin 9	307KHz CMOS 1:1 M/S
U1438 pin 1	5μs negative going pulse every 5ms.
U1438 pin 9	200KHz CMOS 1:1 M/S
U1436 pin 12	2MHz CMOS 1:1 M/S

Instrument in Normal mode.

U1401 pins 22–37	All +5V (Processor "asleep")
U1401 pin 40	1.228MHz CMOS 1:1 M/S
U1401 pin 39	1.228MHz CMOS 1:3 M/S
U1445 pin 9	307KHz CMOS 1:1 M/S

5.4 SETTING UP PROCEDURE

The following procedure details the adjustments necessary to recalibrate the 1425 and set all the preset controls to achieve the specified performance. Inability to make these adjustments or failure to meet the specification after these adjustments have been made, should be considered as a fault and the operating conditions should be checked according to Section 5.3.

Set the Instrument initially to NORMAL mode.

(a) Test Equipment

1. Multirange Test Meter including 2.5kV capability at 20kΩ/Volt.
2. Variable Autotransformer, output voltage 100-270V at 5A.
3. Sine/Square wave signal generator 10Hz to 100kHz, 20mV to 5V.
4. Source of Voltage and Time Calibration signals, such as Bradley Oscilloscope Calibrator type 192.
5. Square Wave Generator at 500kHz, 100mV, amplitude into 50Ω, rise time less than 50ns with square corner and flat top.
6. RF Sinewave Constant Amplitude Signal Generator 25mV to 5V/pk to pk, 50kHz to 20MHz.
7. 10:1 Passive probe.

(b) Set E.H.T.

Set the incoming a.c. supply via the auto transformer to the nominal centre voltage of the selected range. Set to mid brilliance on the c.r.t. Monitor the collector voltage of Q707. Adjust R725 for this voltage to be 405V ±5V. Remove the voltmeter. The instrument may now be operated directly from the uncontrolled supply.

(c) Set Intensity Range

Set to X-Y mode with inputs grounded and centre the spot on the screen. Monitor the collector voltage of Q702. Adjust the intensity control for this voltage to be +13V, and then adjust R713 for the intensity to be near cut-off. Remove the voltmeter.

(d) Astigmatism

Display a mid frequency sinusoidal signal in the normal sweep mode on one channel, approx. 2Div pk to pk, and 4Div period. Set the VARiable sensitivity control fully anti-clockwise. Set to a fairly low brilliance and adjust both the focus control and R708 (Astig) for the sharpest trace over the whole of its length. Reset the VARiable sensitivity to CAL.

(e) Trace Rotation

Ground the inputs and set the horizontal trace to the centre line. Adjust the Trace Rotation preset to align the trace with the centre graticule line.

(f) Timebase Calibration

Ensure that the VARiable sweep is set to the CAL position. Apply 0.1ms calibrated markers to either channel input. Set the timebase to 0.1ms/Div. and obtain a triggered trace. Apply X10 Magnification and set R553 for 10Div spacing between the time markers.

Return to X1 Magnification and set R551 for 1cm spacing.

Apply 1ms/Div markers and set the timebase to 1ms/Div. Set R506 for 1cm spacing between the time markers. All other timebase ranges can be checked for accuracy.

(g) X-Y Calibration

Ensure that the CH1 VARiable sensitivity control is set fully clockwise to CAL. Select X-Y and apply a calibrated 100mV square wave to Channel 1 Input. Select 20mV/Div on CH1, and ground CH2 input. Set R302 for 5cm horizontal trace length.

(h) Channel 1 Calibration
Select CH1. With a 100mV input of 20mV/Div, set R415 for a 5cm vertical amplitude signal. All other sensitivity ranges can be checked for accuracy.

(i) Ensure that the CH2 VARiable sensitivity control is set to the CAL. position. Transfer the 100mV calibration signal to CH2, and set to display that channel at 20mV/Div. Set R352 for a 5cm vertical amplitude signal.

All other sensitivity ramps can be checked for accuracy.

(j) Input Balance
Select CH1 and with input grounded adjust the preset Balance pot for no vertical movement of the trace between the 100mV/Div and the 2mV/Div ranges. Repeat for CH2.

(k) Trigger Balance
Set R357 for no vertical movement of the CH2 trace when Invert is selected. Connect a sinusoidal input, AC coupled, to CH1 and set the trace for about 5Div pk-pk signal, with one cycle displayed. Adjust R307 such that there is no change of trigger point as the TRIGGER Coupling is switched between AC and DC. Note that the relevant Shift control may have to be operated to return the trace to the centre of the screen when R307 or R357 is adjusted.

(l) Add Balance
Ground the inputs to CH1, and CH2 and select DUAL display mode. Using the POSITION centre both traces on the screen. Switch to ADD and adjust R448 to centre the trace on the screen.

(m) Attenuator Compensation
Apply a square wave input to CH1 at approx. 1V pk-pk and 1kHz. Select 0.2V/Div and adjust C109 on the CH1 attenuator assembly to obtain a square topped displayed pulse. Access is through the trim tool hole in the preamplifier screen.

Apply a square wave input to CH1 at approximately 10V pk-pk and 1kHz. Select 2V/Div and adjust C107 on the CH1 attenuator assembly to obtain a square topped displayed pulse.

Repeat for CH2.

(n) Input Capacitance Equalisation
Select 100mV on CH1 with the VARiable Sensitivity control set fully anti-clockwise and monitor a 10V 1kHz square wave via a 10:1 probe. Adjust the capacitive compensation of the probe for a flat topped displayed pulse. Select 200mV/Div, reset the VARiable sensitivity to the CAL position and adjust C102 for a similar Flat top to the pulse.

Select 2V/Div on CH1 with the VARiable Sensitivity control set to the CAL position and monitor a 100V square wave input. Adjust C106 for a flat top to the pulse.

Repeat for CH2.

(o) Pulse Response and Bandwidth
Monitor a fast rise square wave input signal to examine the edge in detail on the 20mV/Div and 0.5μs/Div ranges.

Adjust C405 for a flat top following the transition and C402 for the optimum corner to the pulse.

Connect a constant amplitude sinusoidal generator and set the input for 5cm pk to pk to 50kHz. Increase the frequency and check that the loss of amplitude is less than 3dB at 20MHz (3.5cm pk to pk).

(p) Calibrator
Monitor a calibrated 1V pk to pk square wave input and set the sensitivity and variable sensitivity controls for a full 8cm pk to pk display. Disconnect the external input and connect the Y input to the 1425 Calibrator output. Adjust R641 for a similar 8cm signal amplitude.

(q) Y ADC Adjustment
Select Stored and Refresh mode, cursors on, 0.5ms/div sweep rate and set the display mode to CH1. Apply a 800mV square wave signal to CH1 and select an input attenuator setting of 100mV/div. Set one cursor on a high level and one on a low level. Set R842 mid way and adjust R1329 so the cursor readout displays 800mV. If there is not enough adjustment on R842 adjust R842 as well to give the 800mV cursor reading. Adjust channel shift if cursor reading over-range.

Repeat for CH2, adjusting R1377 ONLY.

(r) Y DAC Adjustment
With the settings as in (r) adjust R821 so that the displayed signal is 8cm in amplitude. Adjust R829, so that the bottom of the cursor readout is 2mm above the bottom graticule line.

(s) Adjustment of pickoff board
Set CH1 input coupling switch to GND. Ensure CH1 trigger is selected and BRIGHT LINE is On. Set NORMAL mode, and 0.5ms/div on the TIME/DIV switch. Adjust the CH1 Y shift control

(i) Switch to STORE mode. If a trace displacement occurs, adjust R1325 to bring the trace back to the centre of the screen.
(ii) Switch back to NORMAL mode and move TRACE to the upper edge of the screen. Return back to STORE mode and adjust

R1323 set the trace at the upper edge of the screen, if necessary.

(iii) Repeat step (i).

Select DUAL mode on the DISPLAY MODE switch.

Select CH2 on the DISPLAY MODE switch and set the CH2 input coupling to GND. Set BRIGHT LINE ONE, CH2 TRIGGER and NORMAL mode.

(i) Adjust the CH1 Y shift control to centre the trace on the screen. Switch to STORE mode and adjust R1374 to centre the trace again.

(ii) Return to NORMAL mode, and shift the trace up to the upper edge of the display. Switch back to STORE mode and adjust R1373 so that the trace is at the upper edge of the screen.

(iii) Repeat step (i).

(t) Adjustment of Sampling Circuitry
Select 20μs/div on the TIME/DIV switch. Set the NORM NORMAL/STORE button to STORE, select CH1 on the DISPLAY MODE switch, and CH1 TRIGGER . Set BRIGHT LINE ON and CH1 input coupling to GND.

Set R838 fully anti-clockwise. Remove U902 and connect pin 12 of the socket to +5V and pins 11, 7, 6, 5, 4, 3 to ground. Operate the ARM control. The display will now go blank. Adjust R838 until a trace appears. R838 should be set as near the point which initiates a trace as possible.

Replace U902.

(u) Digital Timebase adjustment
Apply 1ms markers to CH1 input. Set the TIME/DIV switch to 1ms. Select STORE mode and operate the RELEASE button. Obtain a centred triggered trace and adjust R834 to obtain 1cm spacing between the markers.

NOTE TO SECTION 5.4

The unstabilised EHT voltage is a function of the peak-to-peak supply voltage and is thus waveform dependent. Operation of the set via a variable or other transformer may introduce peak clipping of the supply to the set and cause subsequent errors in checking or re-setting the EHT stabiliser range. (R725 according to section 5.4b above).

To check the effect of introducing a variable transformer to drive the set, first operate the set directly from the supply and note the supply voltage and the collector voltage of Q707.

Then operate the set via the variable transformer and adjust the supply voltage to the set to give the same voltage on Q707. Any difference in the supply voltage as measured represents a limitation of the variable transformer.

For example:-
Assume that when operating directly from the supply, the supply is measured as 250V and the voltage on Q707 as 430V.

Then on operation of the set through a variable transformer, the output of that transformer into the set is measured as 265V when adjusted to give the same 430V on Q707. The difference of 15V is a result of the impedance of the variable transformer. The input to the set should be adjusted to 240V + 15V, (i.e. 255V) to check or set the voltage on Q707 to 405V.

The voltage on Q707 can have an error of ± 20V before any stabilisation problem occurs. Note that adjustment of R725 changes the stabilised EHT voltage and subsequent full recalibration of the set is required. The stabilised EHT voltage should be −1850V ±5%.

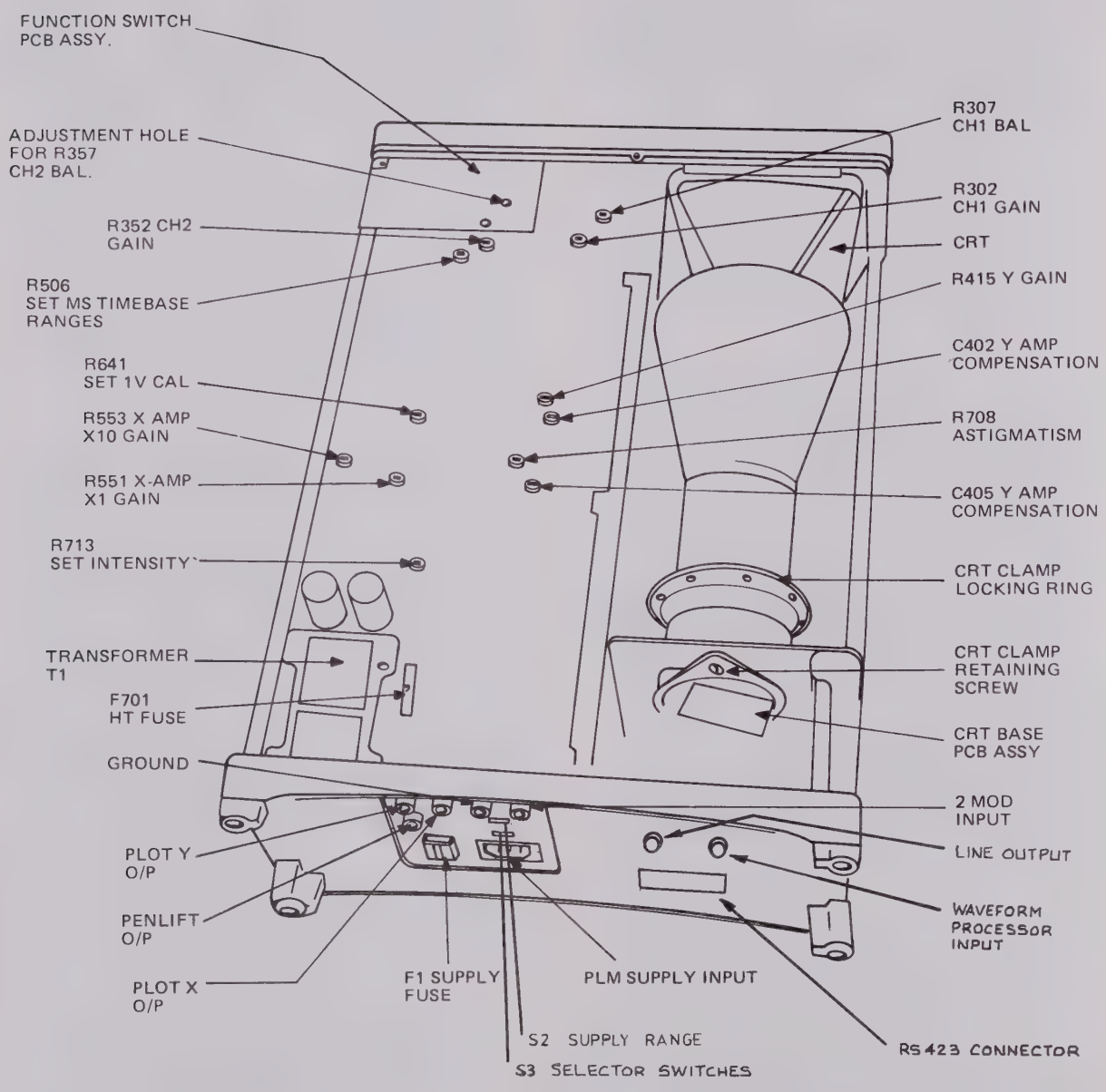


Fig 2A Internal Assembly – Top View

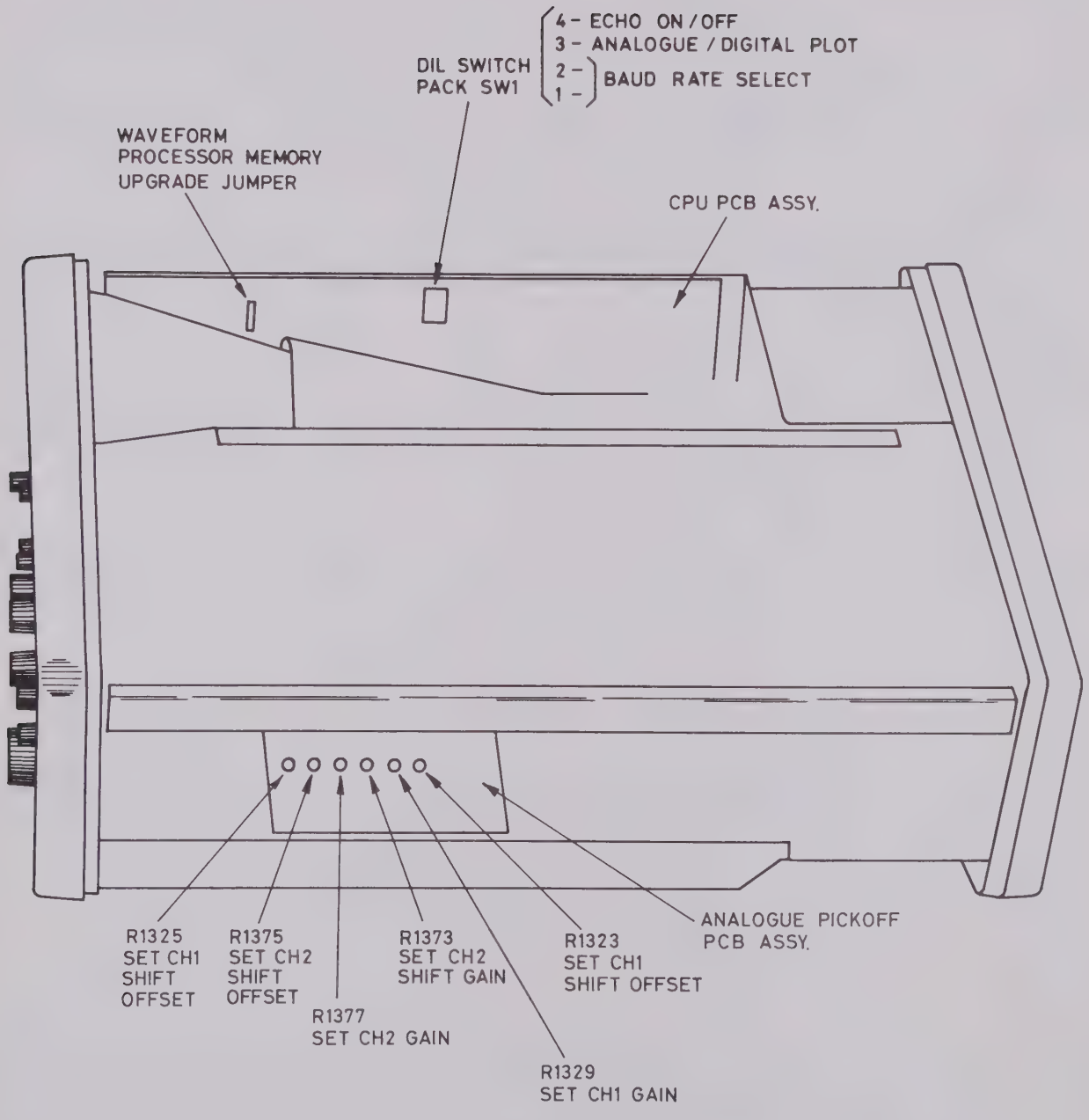

4 - ECHO ON / OFF
3 - ANALOGUE / DIGITAL PLOT
DIL SWITCH PACK SW1
2 -
1 -
BAUD RATE SELECT
WAVEFORM PROCESSOR MEMORY UPGRADE JUMPER
CPU PCB ASSY.
R1325 SET CH1 SHIFT OFFSET
R1375 SET CH2 SHIFT OFFSET
R1377 SET CH2 GAIN
R1373 SET CH2 SHIFT GAIN
R1329 SET CH1 GAIN
R1323 SET CH1 SHIFT OFFSET
ANALOGUE PICKOFF PCB ASSY.

Fig 2B Internal Assembly — Side View

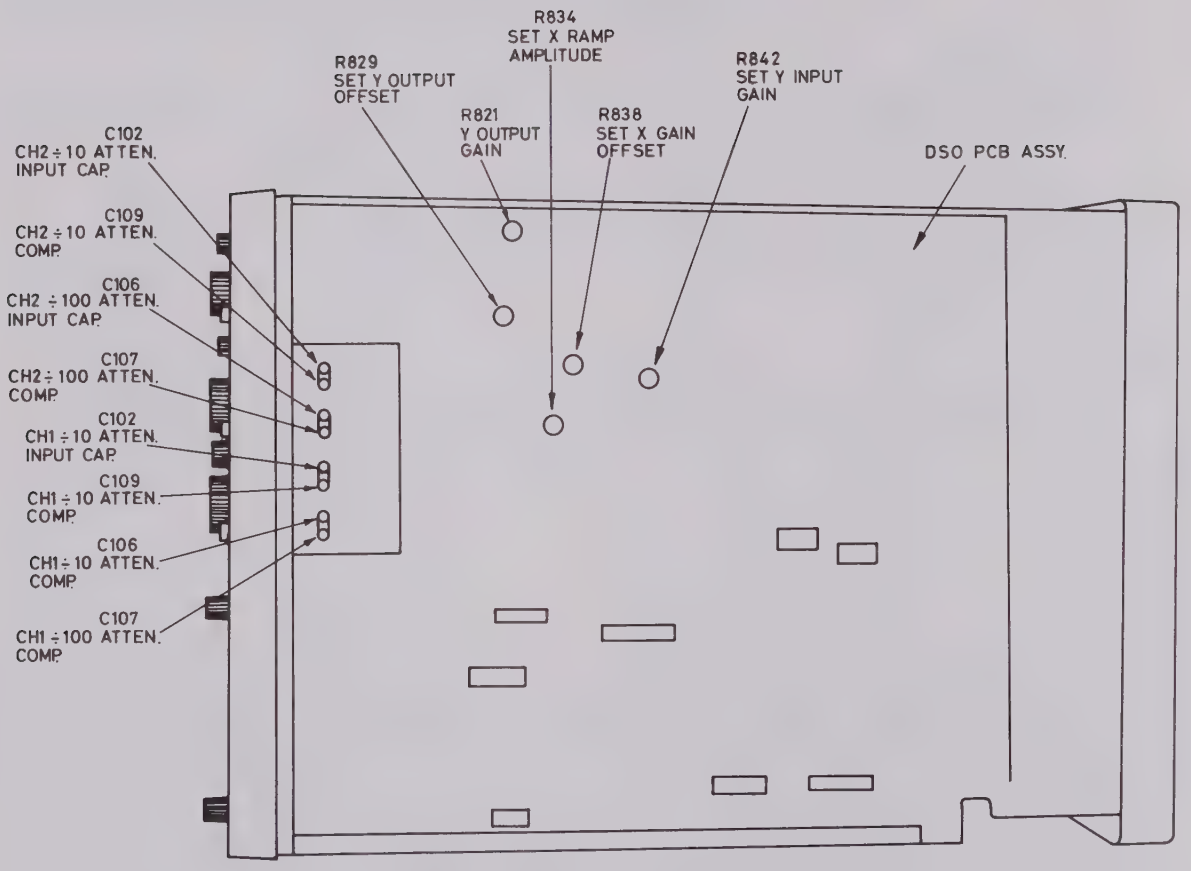
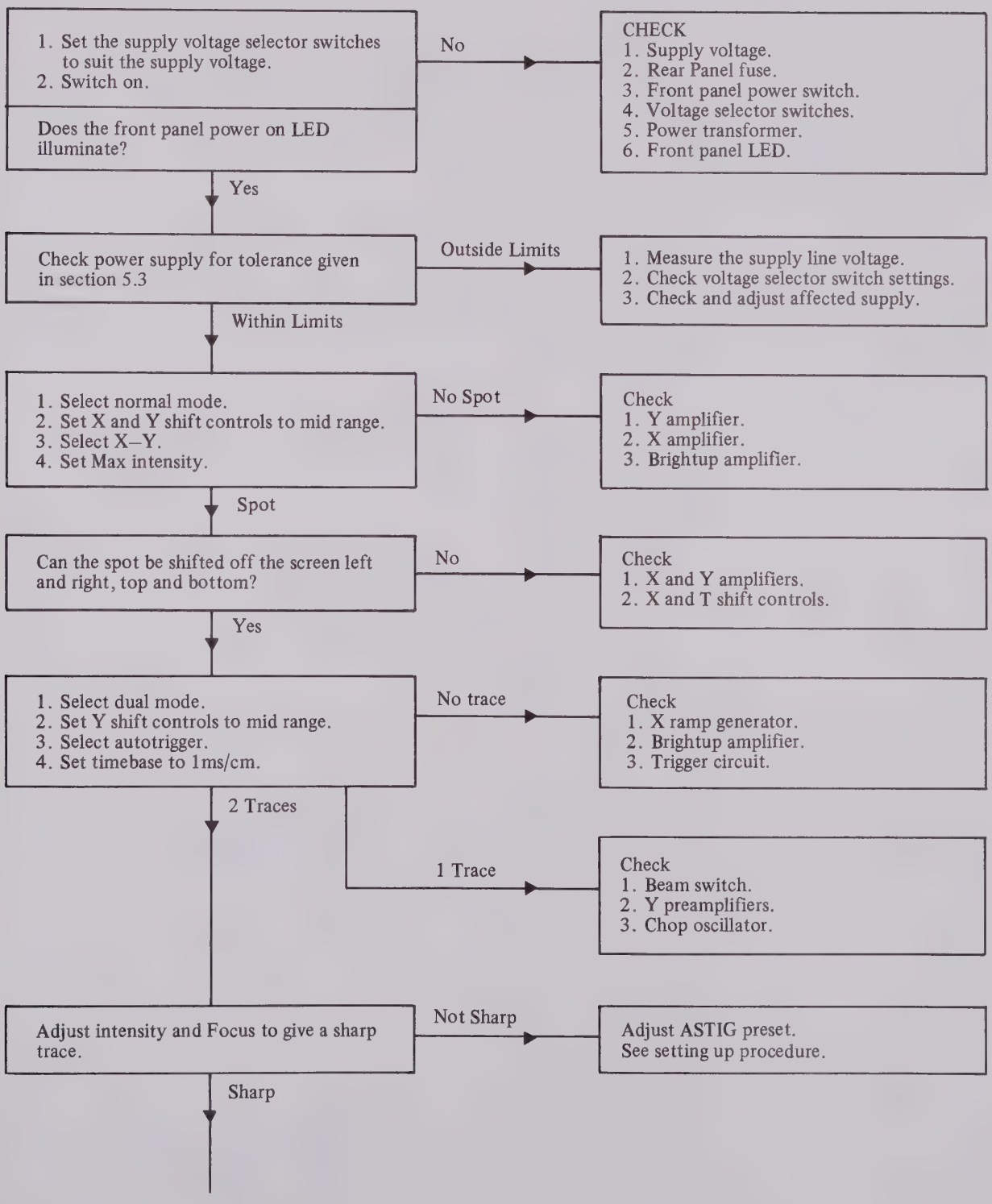
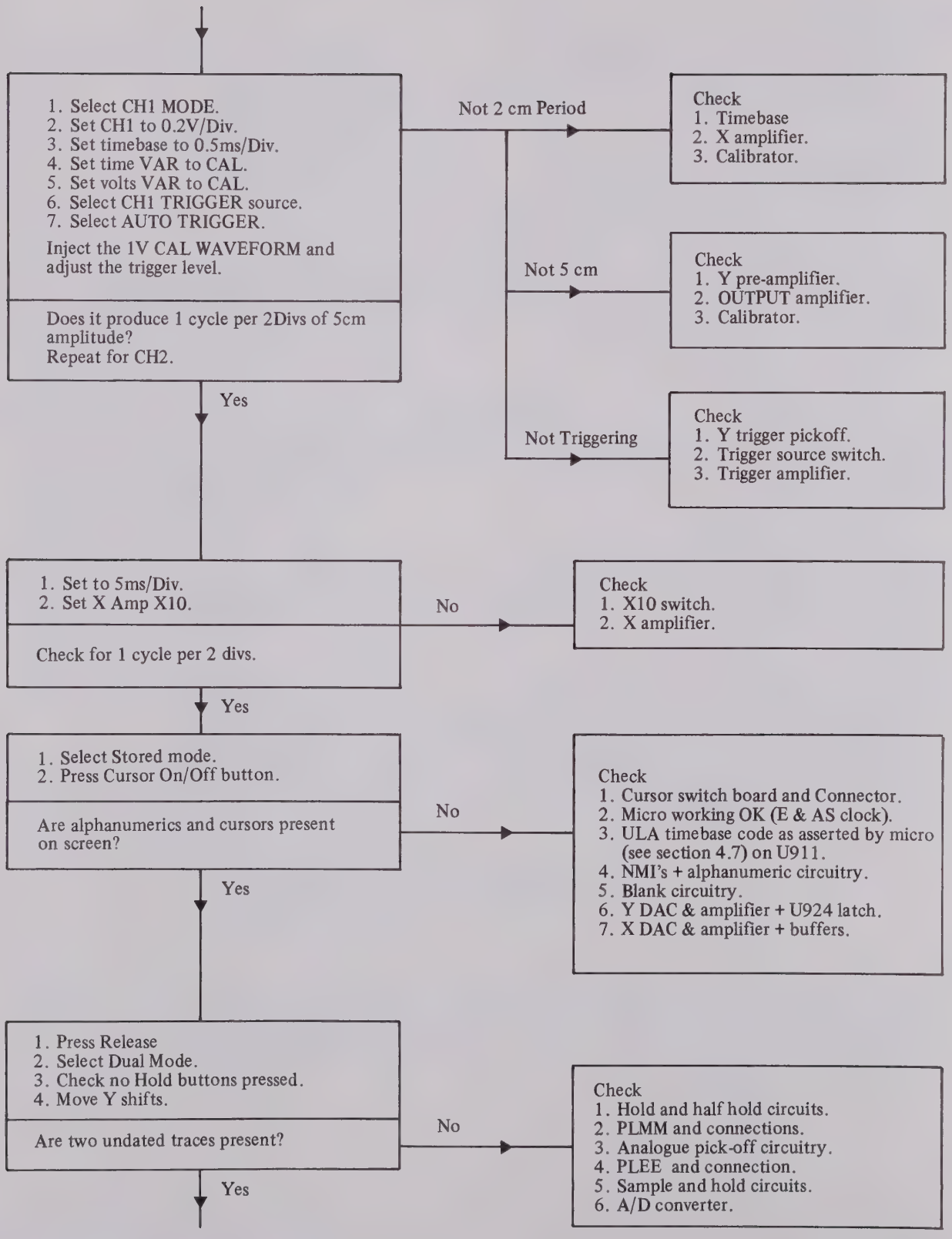
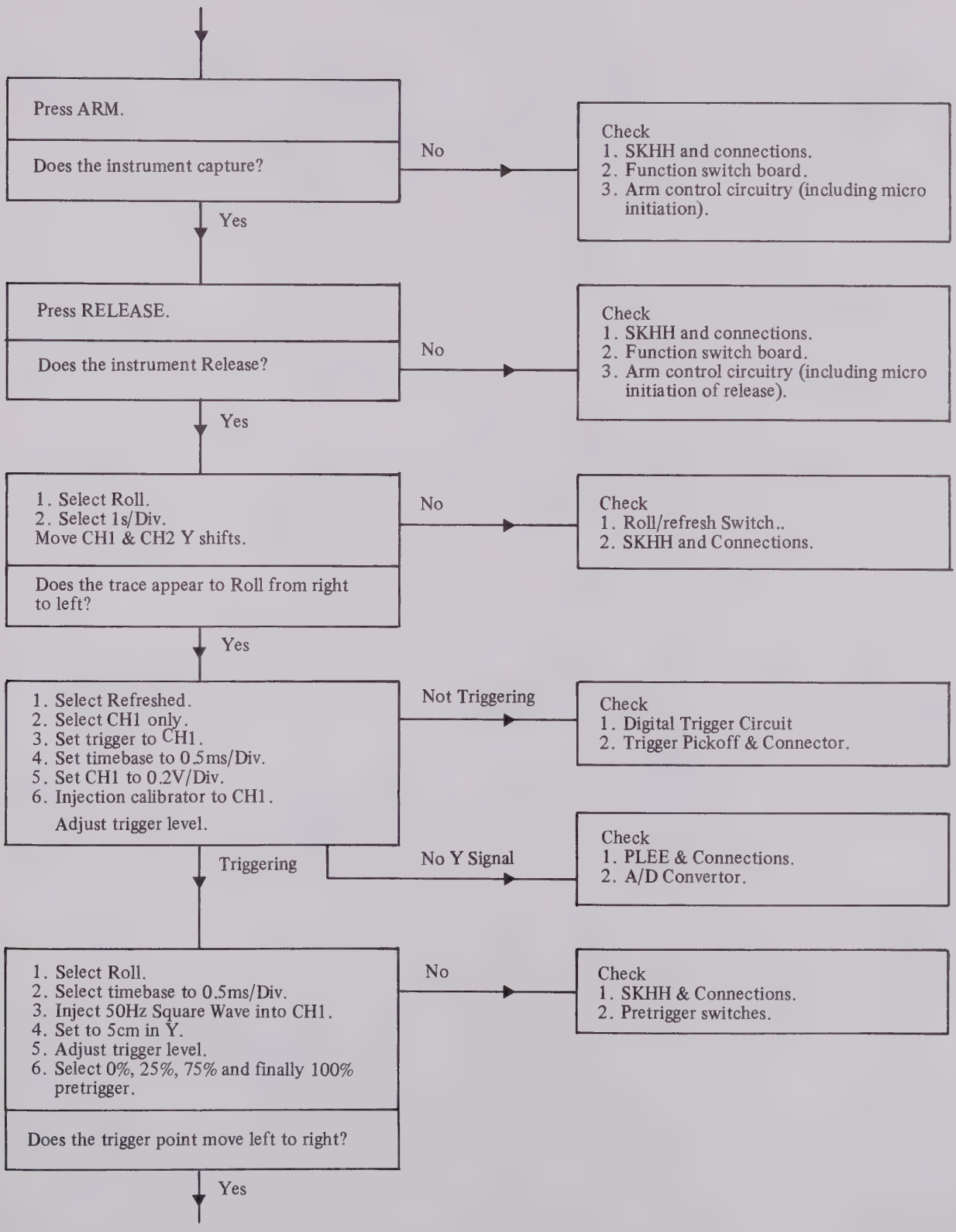


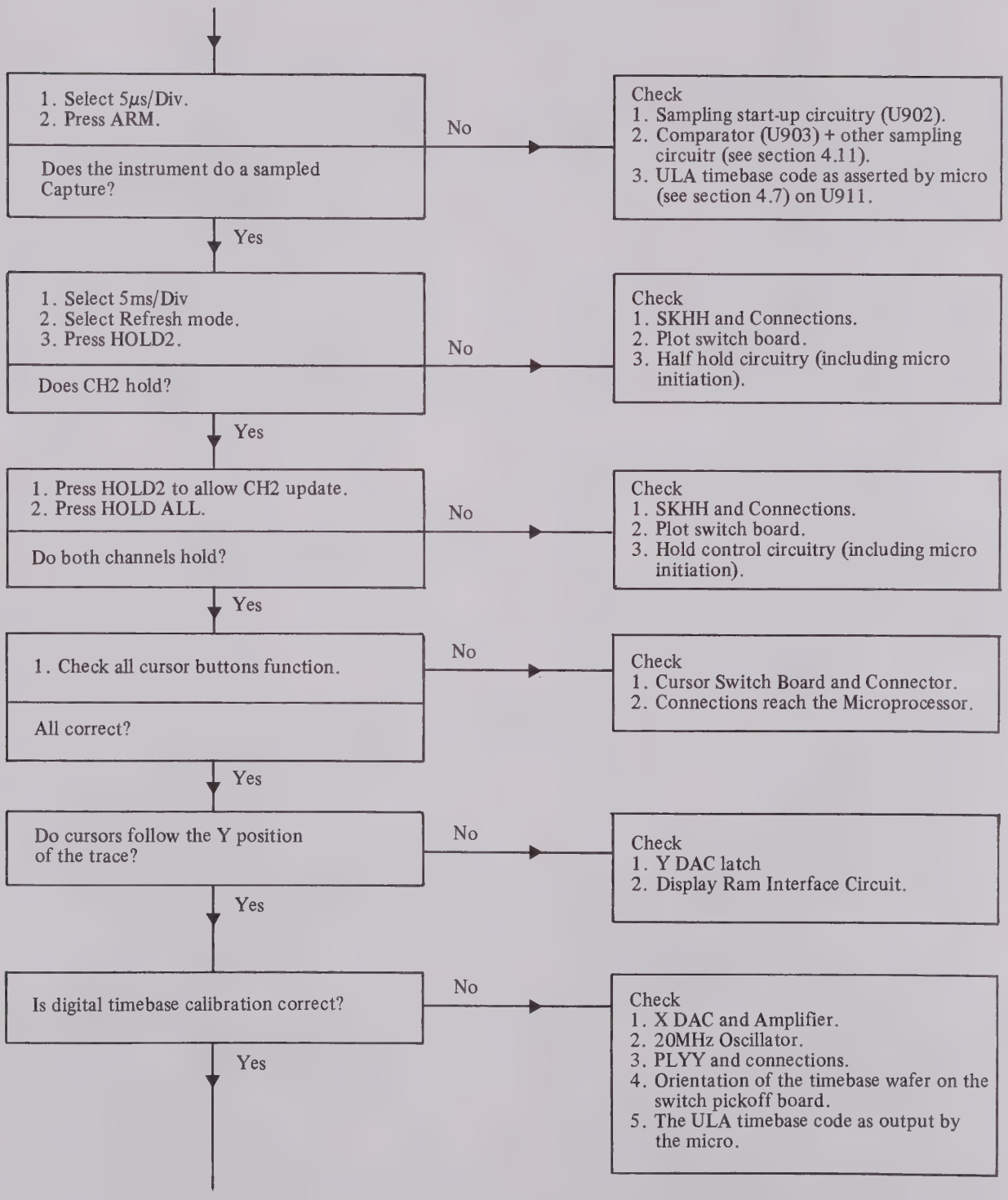
Fig 2C Internal Assembly – Bottom View

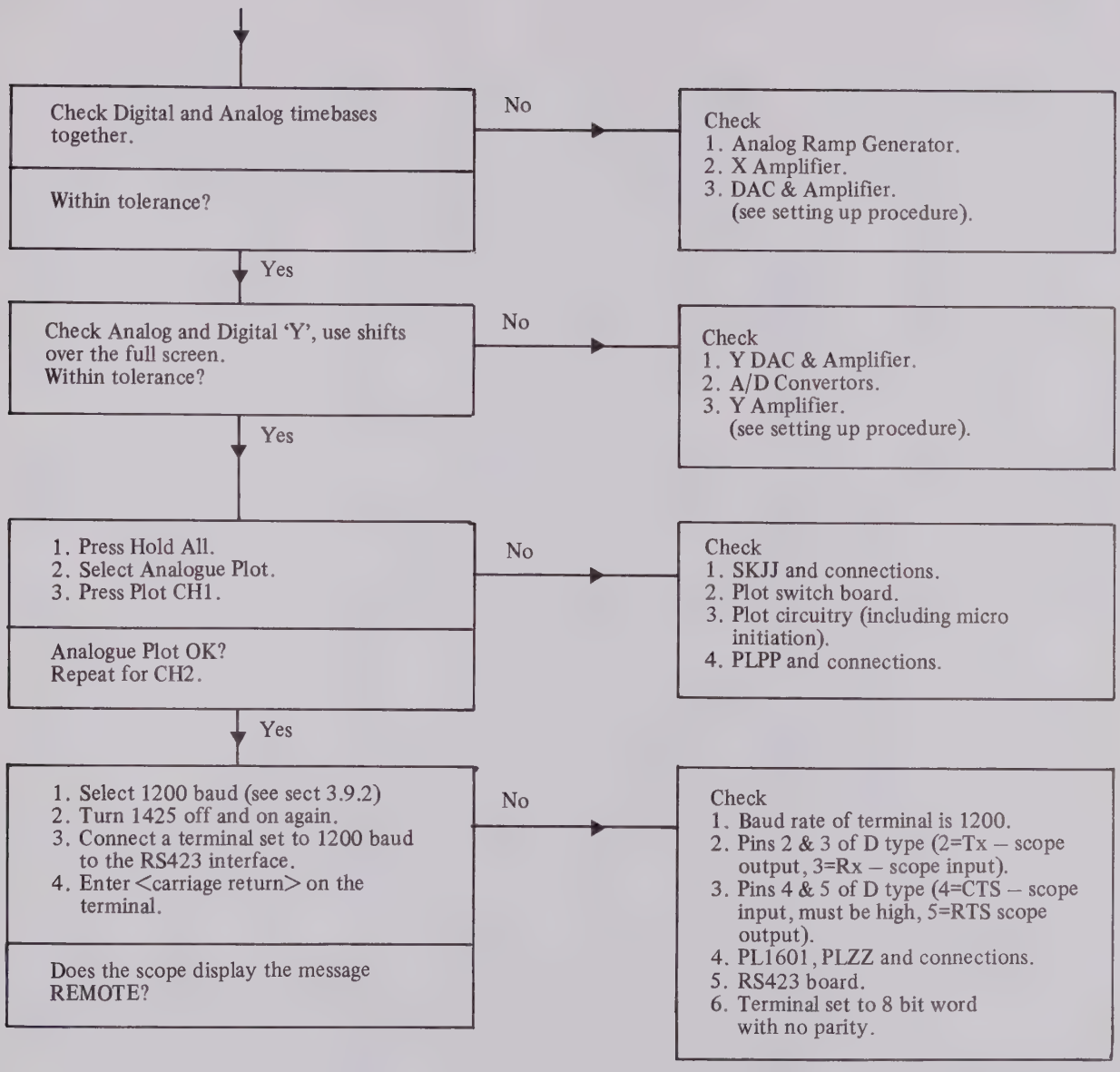
FAULT FINDING




1. Select CH1 MODE.
2. Set CH1 to 0.2V/Div.
3. Set timebase to 0.5ms/Div.
4. Set time VAR to CAL.
5. Set volts VAR to CAL.
6. Select CH1 TRIGGER source.
7. Select AUTO TRIGGER.
Inject the 1V CAL WAVEFORM and adjust the trigger level.
Does it produce 1 cycle per 2Divs of 5cm amplitude?
Repeat for CH2.
Not 2 cm Period
Check
1. Timebase
2. X amplifier.
3. Calibrator.
Not 5 cm
Check
1. Y pre-amplifier.
2. OUTPUT amplifier.
3. Calibrator.
Not Triggering
Check
1. Y trigger pickoff.
2. Trigger source switch.
3. Trigger amplifier.
Yes
1. Set to 5ms/Div.
2. Set X Amp X10.
Check for 1 cycle per 2 divs.
No
Check
1. X10 switch.
2. X amplifier.
Yes
1. Select Stored mode.
2. Press Cursor On/Off button.
Are alphanumerics and cursors present on screen?
No
Check
1. Cursor switch board and Connector.
2. Micro working OK (E & AS clock).
3. ULA timebase code as asserted by micro (see section 4.7) on U911.
4. NMI's + alphanumeric circuitry.
5. Blank circuitry.
6. Y DAC & amplifier + U924 latch.
7. X DAC & amplifier + buffers.
Yes
1. Press Release
2. Select Dual Mode.
3. Check no Hold buttons pressed.
4. Move Y shifts.
Are two undated traces present?
No
Check
1. Hold and half hold circuits.
2. PLMM and connections.
3. Analogue pick-off circuitry.
4. PLEE and connection.
5. Sample and hold circuits.
6. A/D converter.
Yes


Press ARM.
Does the instrument capture?
No
Check
1. SKHH and connections.
2. Function switch board.
3. Arm control circuitry (including micro initiation).
Yes
Press RELEASE.
Does the instrument Release?
No
Check
1. SKHH and connections.
2. Function switch board.
3. Arm control circuitry (including micro initiation of release).
Yes
1. Select Roll.
2. Select 1s/Div.
Move CH1 & CH2 Y shifts.
Does the trace appear to Roll from right to left?
No
Check
1. Roll/refresh Switch..
2. SKHH and Connections.
Yes
1. Select Refreshed.
2. Select CH1 only.
3. Set trigger to CH1.
4. Set timebase to 0.5ms/Div.
5. Set CH1 to 0.2V/Div.
6. Injection calibrator to CH1.
Adjust trigger level.
Not Triggering
Check
1. Digital Trigger Circuit
2. Trigger Pickoff & Connector.
Triggering
No Y Signal
Check
1. PLEE & Connections.
2. A/D Convertor.
1. Select Roll.
2. Select timebase to 0.5ms/Div.
3. Inject 50Hz Square Wave into CH1.
4. Set to 5cm in Y.
5. Adjust trigger level.
6. Select 0%, 25%, 75% and finally 100% pretrigger.
Does the trigger point move left to right?
No
Check
1. SKHH & Connections.
2. Pretrigger switches.
Yes


1. Select 5μs/Div.
2. Press ARM.
Does the instrument do a sampled Capture?
No
Check
1. Sampling start-up circuitry (U902).
2. Comparator (U903) + other sampling circuitr (see section 4.11).
3. ULA timebase code as asserted by micro (see section 4.7) on U911.
Yes
1. Select 5ms/Div
2. Select Refresh mode.
3. Press HOLD2.
Does CH2 hold?
No
Check
1. SKHH and Connections.
2. Plot switch board.
3. Half hold circuitry (including micro initiation).
Yes
1. Press HOLD2 to allow CH2 update.
2. Press HOLD ALL.
Do both channels hold?
No
Check
1. SKHH and Connections.
2. Plot switch board.
3. Hold control circuitry (including micro initiation).
Yes
1. Check all cursor buttons function.
All correct?
No
Check
1. Cursor Switch Board and Connector.
2. Connections reach the Microprocessor.
Yes
Do cursors follow the Y position of the trace?
No
Check
1. Y DAC latch
2. Display Ram Interface Circuit.
Yes
Is digital timebase calibration correct?
No
Check
1. X DAC and Amplifier.
2. 20MHz Oscillator.
3. PLYY and connections.
4. Orientation of the timebase wafer on the switch pickoff board.
5. The ULA timebase code as output by the micro.
Yes


Check Digital and Analog timebases together.
Within tolerance?
No
Check
1. Analog Ramp Generator.
2. X Amplifier.
3. DAC & Amplifier.
(see setting up procedure).
Yes
Check Analog and Digital 'Y', use shifts over the full screen.
Within tolerance?
No
Check
1. Y DAC & Amplifier.
2. A/D Convertors.
3. Y Amplifier.
(see setting up procedure).
Yes
1. Press Hold All.
2. Select Analogue Plot.
3. Press Plot CH1.
Analogue Plot OK?
Repeat for CH2.
No
Check
1. SKJJ and connections.
2. Plot switch board.
3. Plot circuitry (including micro initiation).
4. PLPP and connections.
Yes
1. Select 1200 baud (see sect 3.9.2)
2. Turn 1425 off and on again.
3. Connect a terminal set to 1200 baud to the RS423 interface.
4. Enter <carriage return> on the terminal.
Does the scope display the message REMOTE?
No
Check
1. Baud rate of terminal is 1200.
2. Pins 2 & 3 of D type (2=Tx – scope output, 3=Rx – scope input).
3. Pins 4 & 5 of D type (4=CTS – scope input, must be high, 5=RTS scope output).
4. PL1601, PLZZ and connections.
5. RS423 board.
6. Terminal set to 8 bit word with no parity.

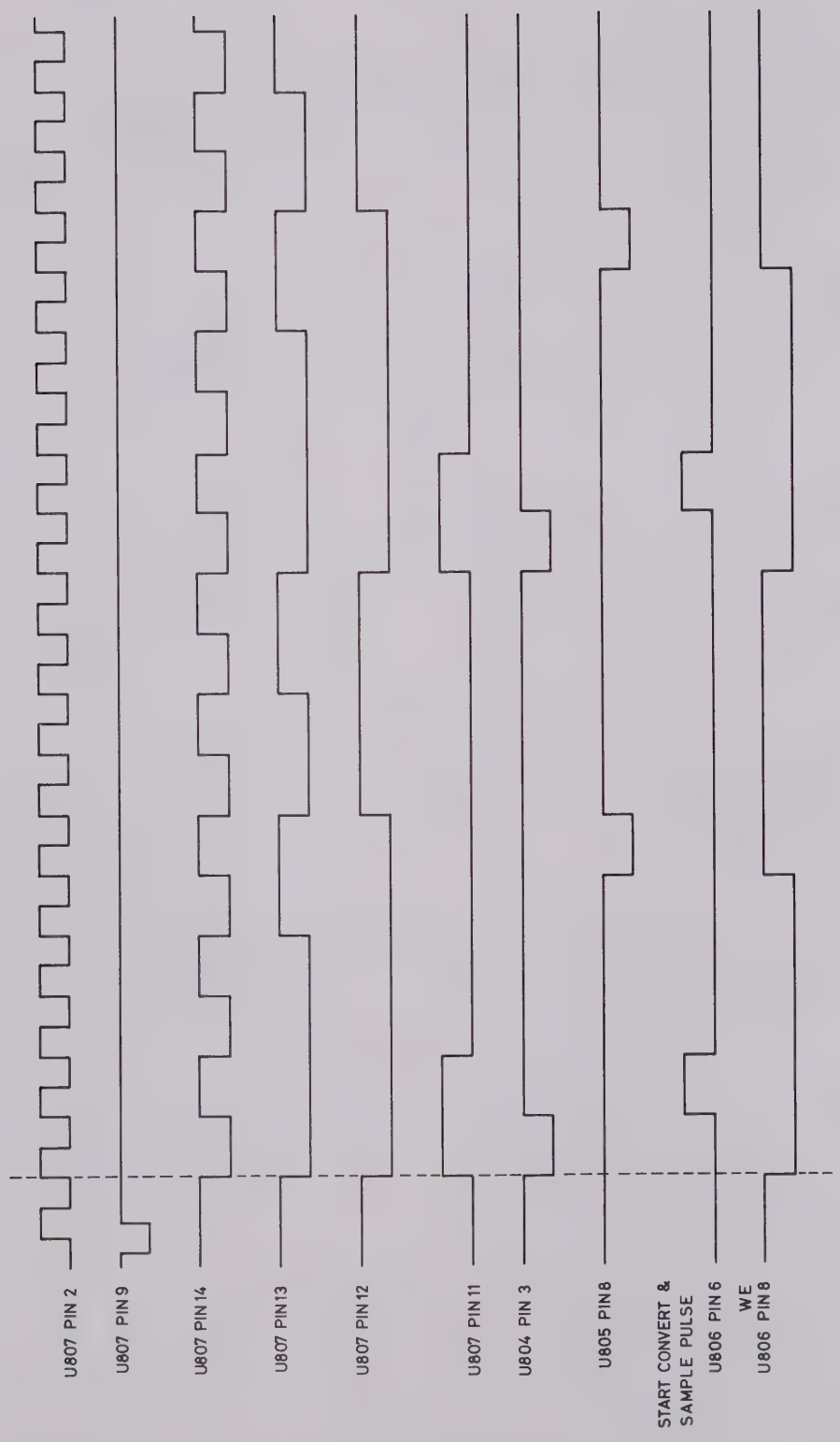


Fig. 3 Control & Timing Logic Waveforms

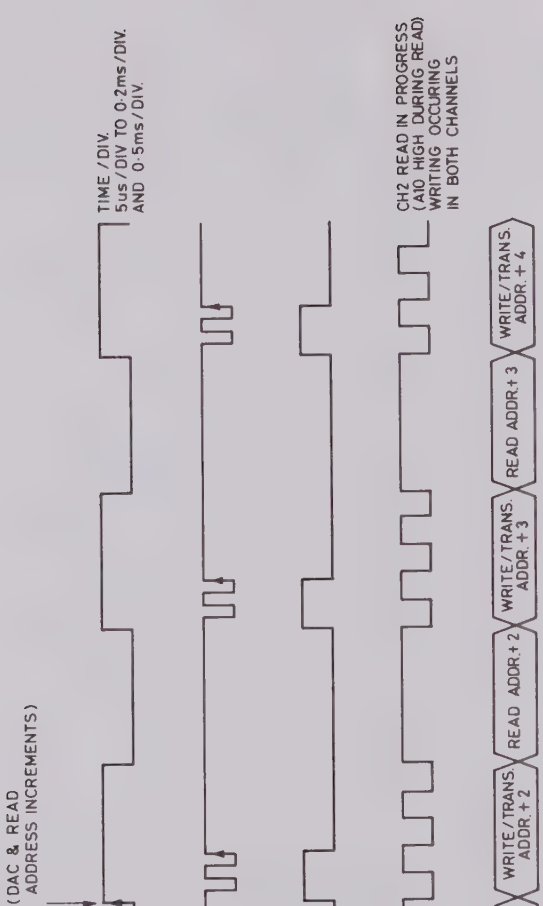


Fig. 4 Write/Transfer Timing Diagram

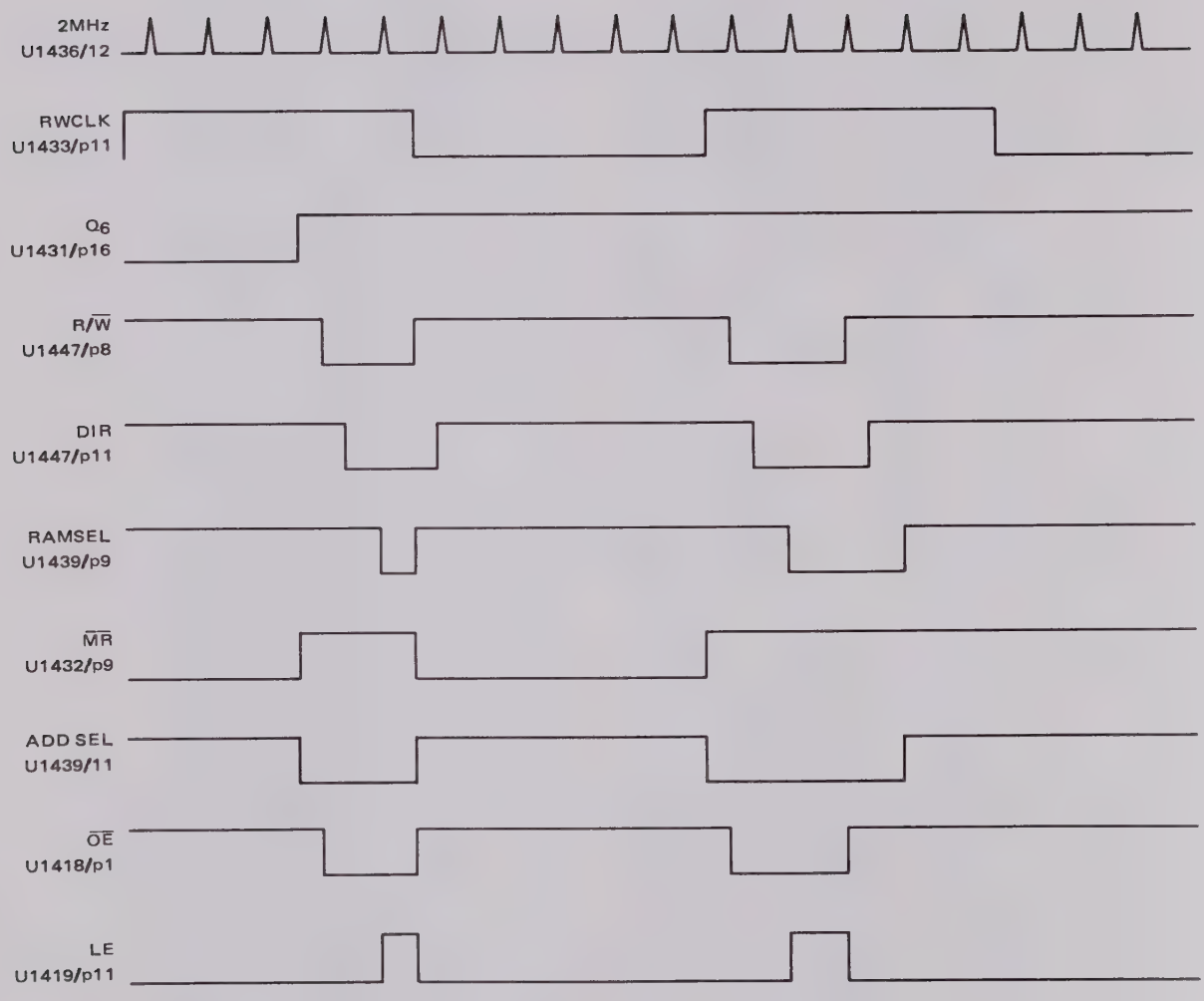
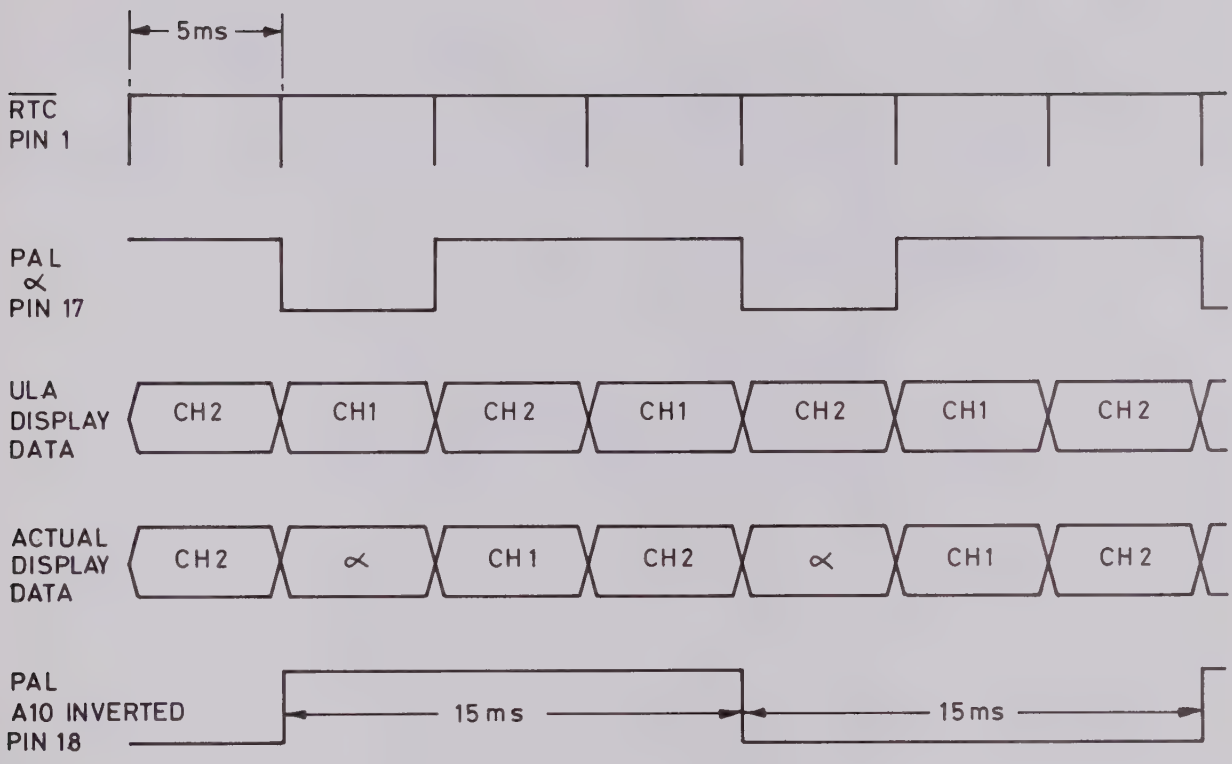


Fig. 5A CPU to DSO RAM Interface Timing Diagram



NOT TRUE FOR RANGES 0·2ms/DIV. TO 0·05ms/DIV.

Fig. 5B Pal Timing

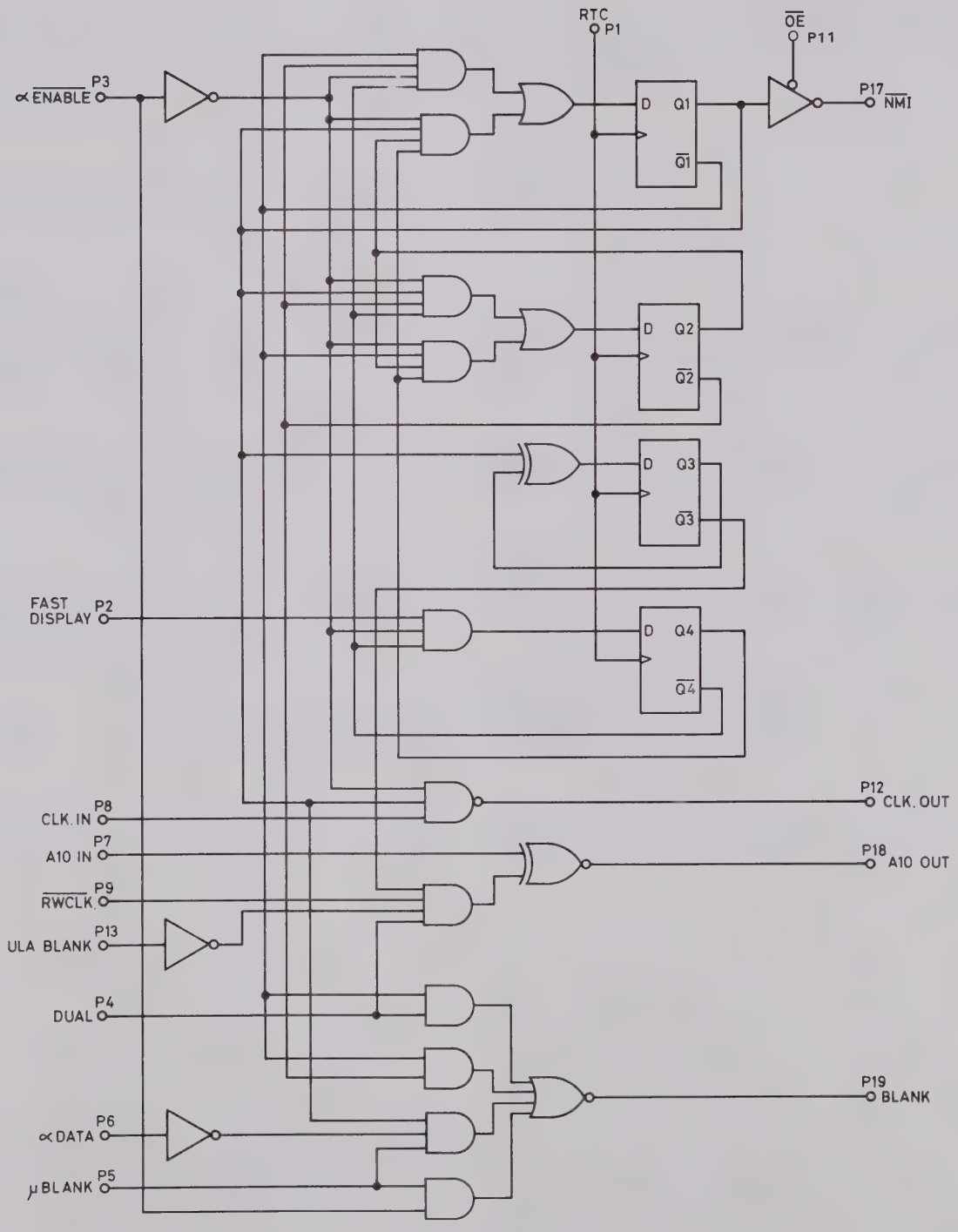


Fig. 5C Pal Functional Diagram

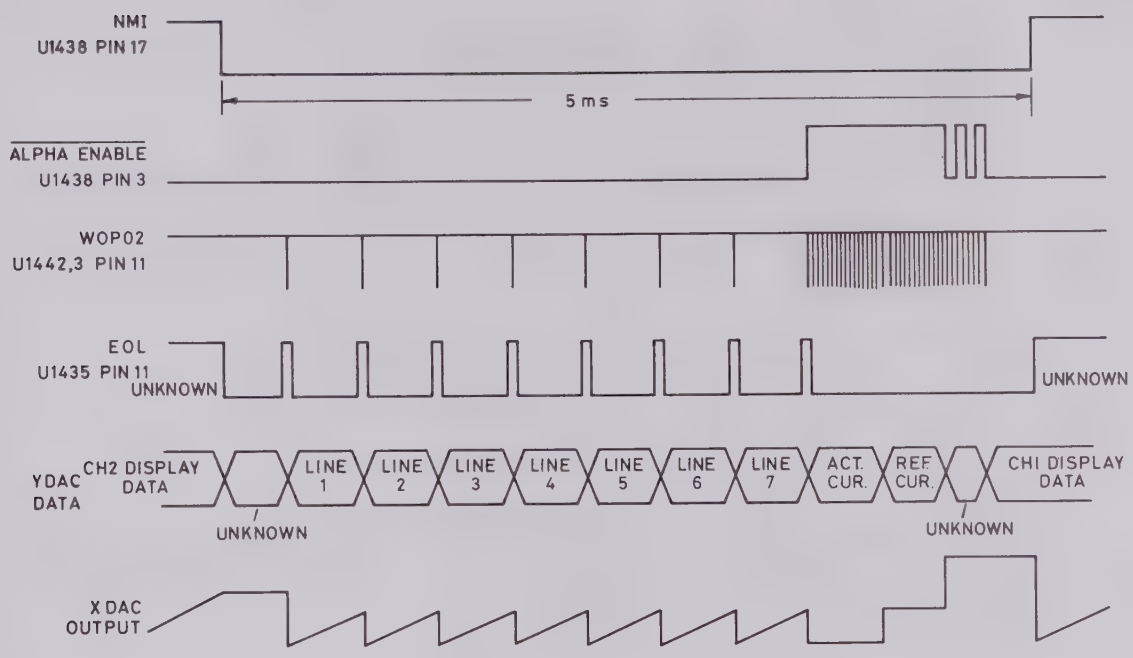


Fig. 5D Alphanumerics & Cursor Display Timings

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	¼W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potenitometer Type MPD, PC		20%	unless otherwise stated
MG	Metal Glaze ½W		5%	unless otherwise stated

CAPACITORS

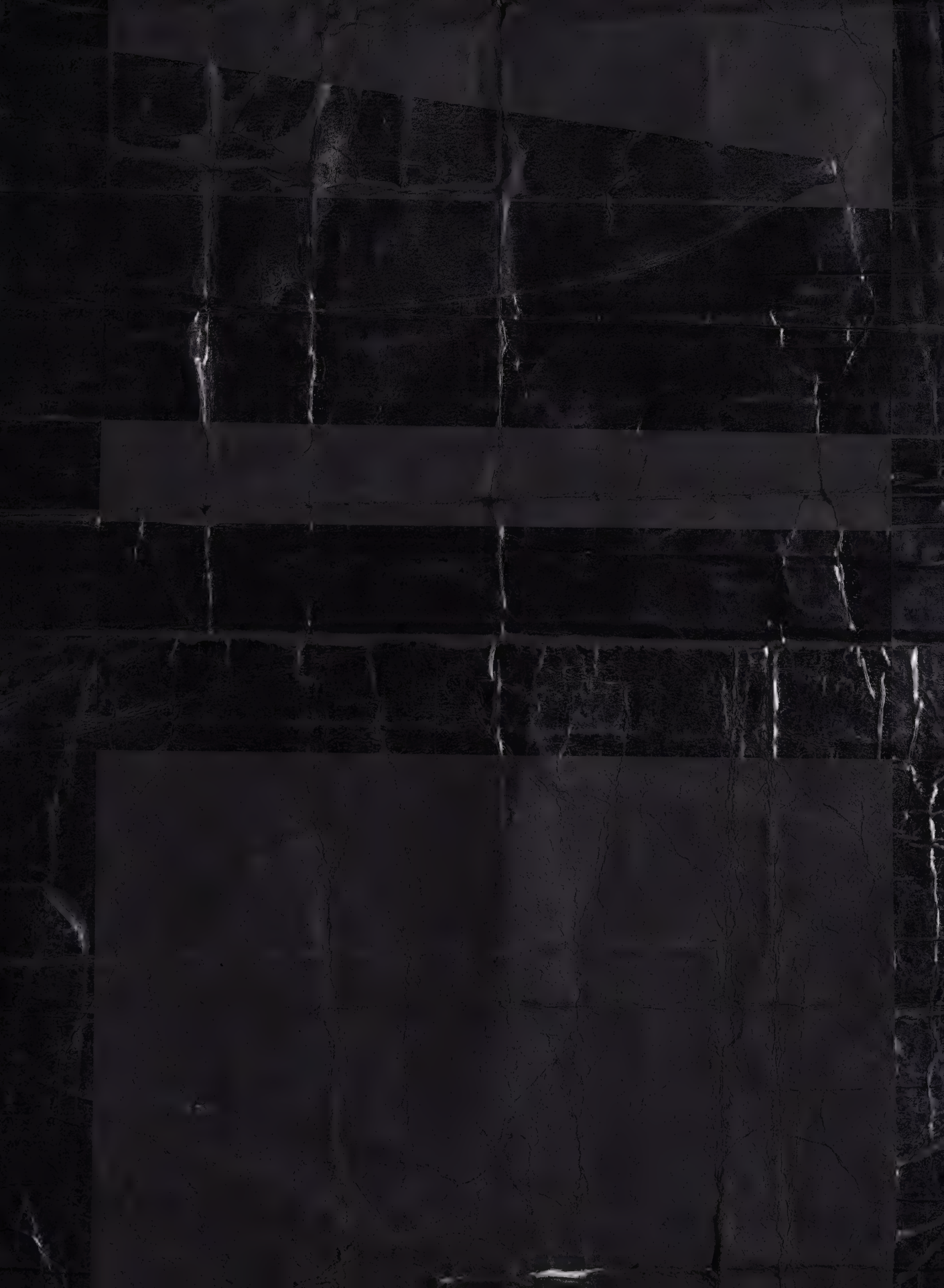
CE(1)	Ceramic		+80% -25%	
CE(2)	Ceramic	500V	±10%	unless otherwise stated
CE(3)	Ceramic	50V		unless otherwise stated
MF	Metallised Film	100V		unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		±10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		±10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (Aluminium)		+50% -10%	
T	Tantalum		+50% -10%	

INTERCONNECTION DIA.

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R744		SHOWN ON SK2980			
R745		SHOWN ON SK2980			
R1101	1k	CF			21799
R1102	390	CF			28722
R1103	4k7	CF			21805
R1104	470k	CF			32330
R1105	10k	CF			21809
R1106	270k	CF			32356
R1107	330k	CF			32357
R1108	470k	CF			32330
R1109	4k7	CF			21805
R1110	100k	CF			21819
R1111	10k	CF			21809
CAPACITORS					
C1101	100nF	CE(3)			43498
C1102	10nF	CE(3)		25V	450548
C1103	10nF	CE(3)		25V	450548
C1104	470nF	CE(3)			43500
C1105	100nF	CE(3)			43498
C1106	10nF	CE(3)		25V	450548

Ref	Value	Description	Tol %	Part No
DIODES				
D1				453840
D704		SHOWN ON SK29		
D1101		L.E.D.		43847
TRANSISTORS				
Q1101		MPS2369		36625
INTEGRATED CIRCUITS				
U1101		74C221		31267
U1102		M75551PA		31317
SWITCHES				
S1101–S1106				30750
S1401–S1405				30179
MISCELLANEOUS				
V1		CRT 56840GY/93		30926

| | | |



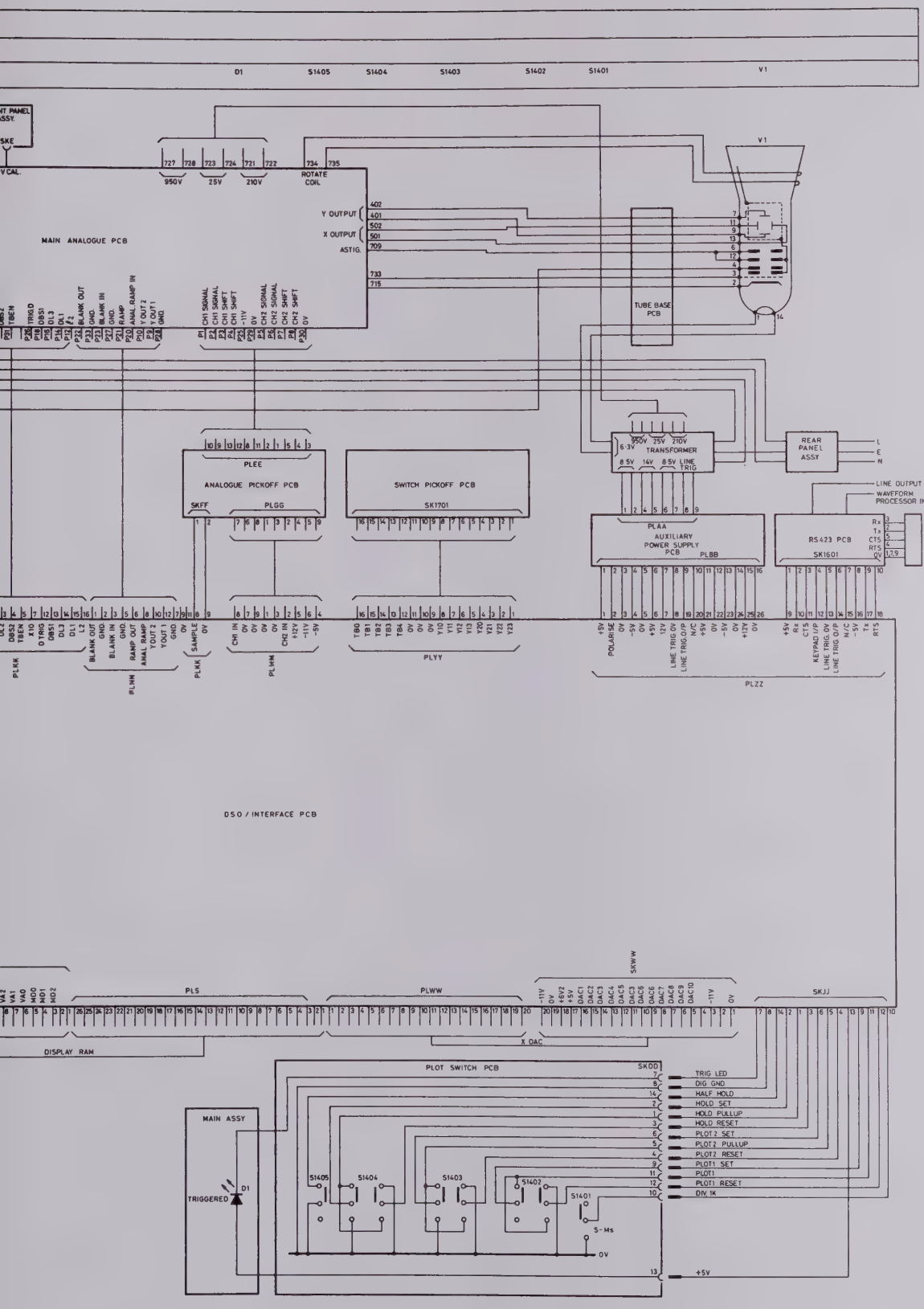


Fig. 6 Interconnection Circuit Diagram

1425 MAIN BOARD, TIMEBASE & TRIGGER AND POWER SUPPLY (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R572	22k	CF			21812
R573	4k7	CF			21805
R574	12k	CF		1W	19051
R575	12k	CF		1W	19051
R576	10k	MO	5		44987
R577	10k	MO	5		44987
R578	470	CF			21797
R600	22k	CF			21812
R601	27k	CF			21813
R603	3k3	CF			21803
R604	4k7	CF			21805
R605	2k2	CF			21802
R606	27k	CF			21813
R607	2k2	CF			21802
R608	4k7	CF			21805
R609	470	CF			21797
R610	10	CF			21793
R611	680	CF			28723
R612	680	CF			28723
R613	68k	CF			21816
R614	10	CF			21793
R615	12k	CF			21810
R616	470	CF			21797
R617	2k7	CF			28726
R618	47k	CF			21815
R619	3k3	CF			21803
R620	1M	CF			31840
R621	3k3	CF			21803
R622	1k8	CF			28725
R623	150k	CF			21821
R624	10	CF			21793
R626	1M	CF			31840
R627	680k	CF			31839
R628	1M	CF			31840
R629	1M	CF			31840
R630	100k	CF			21819
R631	33k	CF			21814
R632	300k	MF	2		38653
R633	18k	CF			21811
R634	6k8	CF			21807
R635	10	CF			21793
R636	68k	CF			21816
R637	2k2	CF			21802
R638	3k9	CF			21804
R639	10k	CF			21809
R640	39k	CF			28728
R641	2k2	PCP			36265
R642	56k	CF		1W	19058
R643	470	CF			21797
R644	3k3	CF			21803
R645	10k	CF			21809
R701	1k	CF			21799
R702	680	CF			28723
R703	10k	CF		1W	2882
R704	22k	CF			21812
R705	5k6	CF			21806
R706	470	CF			21797
R707	8k2	CF			21808
R708	220k	PCP			36270
R710	2k2	CF			21802
R713	470k	PCP			36271
R714	1M5	CF		½W	454532
R715	680	CF		1/8W	454533
R716	33M	MG	5	½W	43008
R717	33M	MG	5	½W	43008
R718	22k	CC		¼W	3433
R719	18k	CF		½W	18565
R721	180	CF		½W	18541
R722	1k	CF			21799
R723	2k2	CF			21802
R724	5k6	CF			21806
R725	47k	PCP			38261
R726	33k	MF	2		38630
R727	150	CF			28719
R728	68	CF			28716
R729	680	CF			28723
R730	470	CF			21797
R731	10k	CF	2		38618
R732	47k	CF			21815
R733	22k	CC		¼W	3433
R734	68	CF	A.O.T.		28716
R735	1k5	CF			21801
R736	1k	CF			21799
R737	10k	PCP			44959
R738	180	MF	2		38576
R739	47	CF		½W	18534
R741	5k6	CF		1W	2363
R742	220k	MF	2		38650
R743	33M	MG	5	½W	43008
R744	1M	PCP			453626
R745	10k	PCP	(With S1)		453627
R746	82k	CF			21818
R747	120k	CF			21820
R748	100k	CF			21819
R750	1k2	CF			21800
R751	33k	CF			21814
R752	270k	CF			32356
N102		Resistor Network			453399
N261		Resistor Network			38692
N720		Resistor Network			44608

1425 MAIN BOARD, TIMEBASE & TRIGGER AND POWER SUPPLY (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS					
C102		Trimmer			451979
C103		Not Fitted			
C104	68pF	CE(2)			22374
C105	100nF	MF		400V	44966
C106		Trimmer			451979
C107		Trimmer			451979
C108	680pF	PC		160V	40631
C109		Trimmer			451979
C133		Not Fitted			
C135	100nF	MF		400V	44966
C151	10pF	CE(3)			22364
C201	10µF	E		25V	32180
C202	10nF	CE(3)		25V	450548
C203	2.2nF	CE(2)			22389
C204	1nF	CE(3)			42432
C231	10µF	E		25V	32180
C232	10nF	CE(3)		25V	450548
C233	2.2nF	CE(2)			22389
C234	1nF	CE(3)			42432
C263	1.2nF	PS		63V	450536
C264	1µF	PE		100V	41743
C265	10nF	CE(3)		25V	450548
C266	0.1µF	MF		100V	37018
C267	10nF	CE(3)		25V	450548
C268	10nF	CE(3)		25V	450548
C269	15pF	CE(2)			22366
C270	15pF	CE(2)			22366
C271	10nF	CE(3)		25V	450548
C301	10nF	CE(3)		25V	450548
C302	10nF	CE(3)		25V	450548
C303	100nF	CE(3)			43498
C304	22pF	CE(3)			42412
C351	10nF	CE(3)		25V	450548
C352	10nF	CE(3)		25V	450548
C353	39pF	CE(3)			42415
C354	15pF	CE(3)			42410
C401	10nF	CE(3)		25V	450548
C402	60pF	Trimmer			30286
C403	15pF	CE(3)	10		42410
C404	15pF	CE(3)	10		42410
C405	60pF	Trimmer			30286
C406		Not Fitted			
C407	100nF	MF		100V	37018
C408	3.3nF	CE(3)	20		42438
C409	3.3nF	CE(3)	20		42438
C410		Not Fitted			
C411	5.6nF	CE(2)			22394

Ref	Value	Description	Tol %±	Rating	Part No
C413	1nF	CE(3)	10		42432
C501	0.22µF	MF		100V	44370
C502	0.1nF	CE(3)			42432
C503	10nF	CE(3)		25V	450548
C504	10nF	CE(3)		25V	450548
C505		Not Fitted			
C506	10pF	CE(3)			42408
C507	10nF	CE(3)		25V	450548
C508	10nF	CE(3)		25V	450548
C509	100µF	E		16V	450582
C510	0.560pF	CE(3)			42429
C511	3.3nF	CE(3)			42435
C512	5.6nF	CE(2)			22394
C513	100µF	E		16V	450582
C514	330pF	CE(3)			452161
C515	150pF	CE(3)			42422
C516	0.220pF	CE(3)			42424
C519	10nF	CE(3)		25V	450548
C520	10µF	E		25V	32180
C521	22pF	CE(3)			42412
C601	220nF	MF		250V	39201
C602	100pF	CE(3)			42420
C603	2.2µF	E		63V	32194
C604	2.2µF	E		100V	452247
C605	22pF	CE(3)			42412
C606	100nF	MF		100V	37018
C607	100nF	MF		100V	37018
C608	0.22µF	PE		100V	44370
C609	100nF	MF		100V	37018
C610	10nF	CE(3)		25V	450548
C611	22pF	CE(3)			42412
C612	100nF	MF		100V	37018
C613	10nF	CE(3)		25V	450548
C614	47pF	CE(3)			42416
C615	100nF	MF		100V	37018
C616	47µF	E		10V	450581
C617	47nF	MF		100V	39192
C618	47nF	MF		100V	39192
C619	100pF	CE(3)			42420
C620	10nF	CE(3)		25V	450548
C621	10nF	CE(3)		25V	450548
C622	2.2µF	E		63V	32194
C625	100nF	CE(3)			43498
C701	10nF	CE(3)		25V	450548
C702	2200pF	PE		4Kv	44990
C703	2200pF	PE		4Kv	44990
C704	1000µF	E		40V	44992
C705	33µF	E		350V	44991
C708	10µF	E		25V	32180
C709	5.6nF	PE		4Kv	43117

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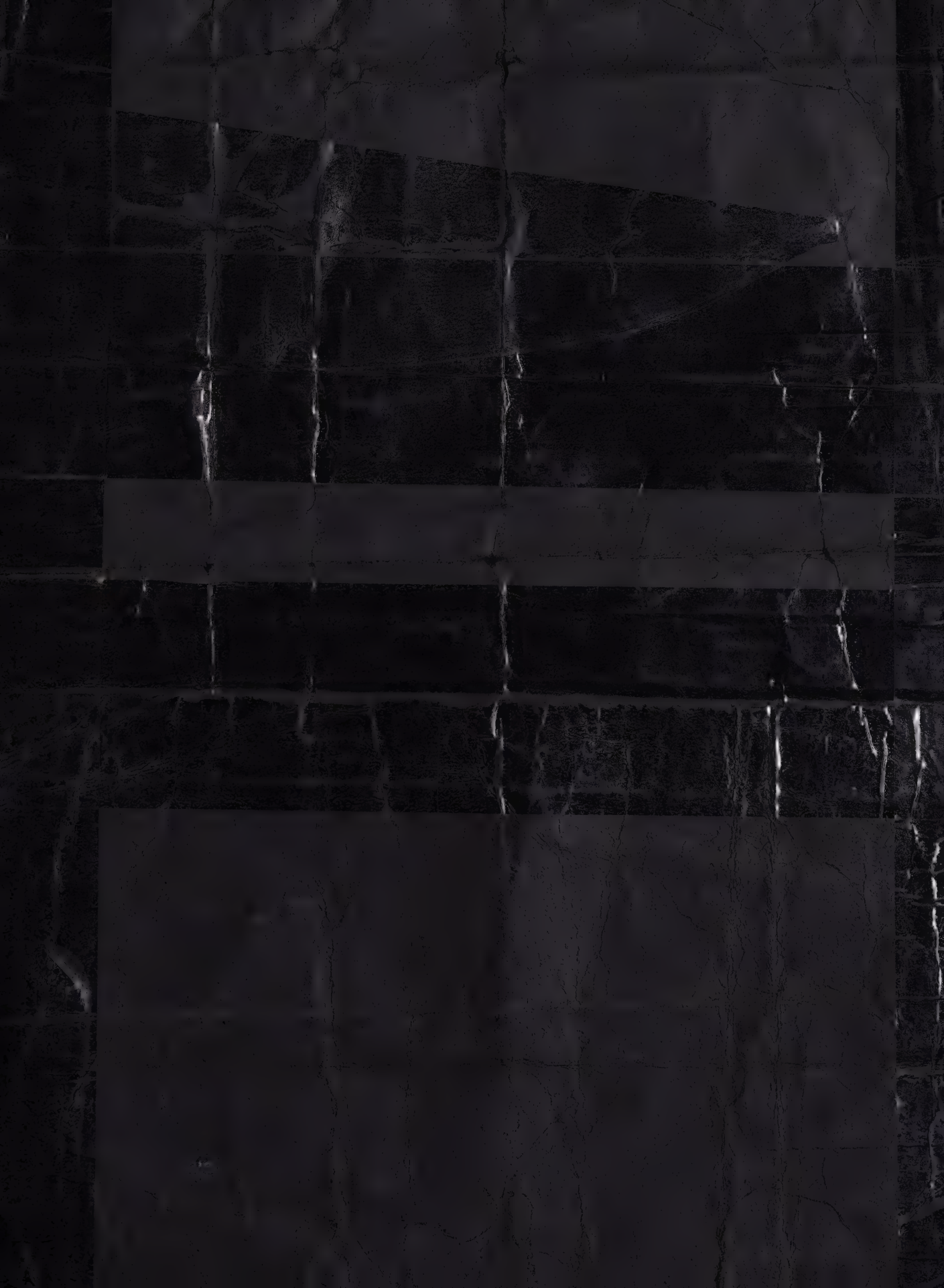
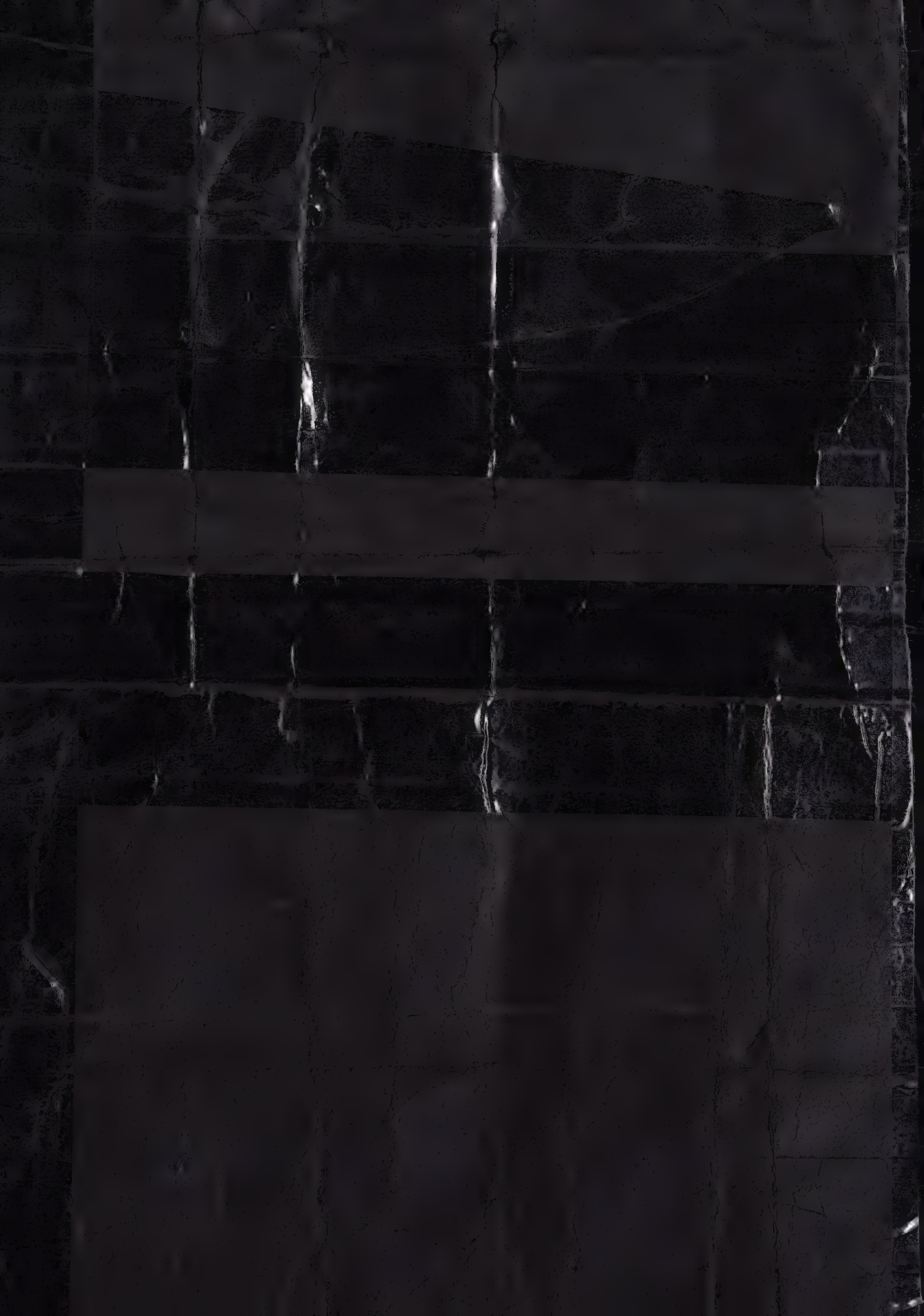
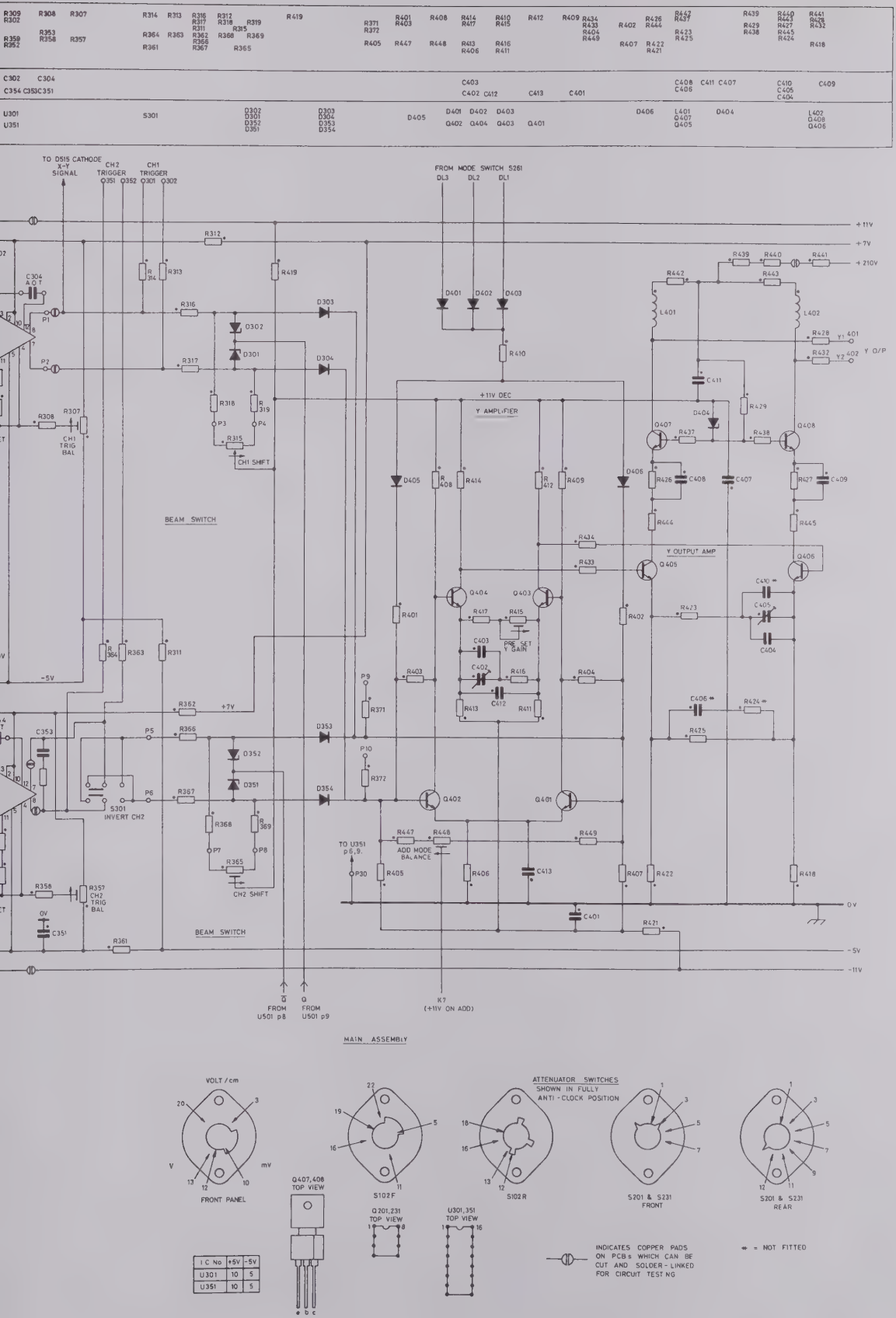






VOLT / cm
FRONT PANEL
Q407, 408 TOP VIEW
S102F
Q201, 231 TOP VIEW
U301, 351 TOP VIEW
ATTENUATOR SWITCHES SHOWN IN FULLY ANTI-CLOCK POSITION
S102R
S201 & S231 FRONT
S201 & S231 REAR
INDICATES COPPER PADS ON PCBs WHICH CAN BE CUT AND SOLDER-LINKED FOR CIRCUIT TESTING
* = NOT FITTED

I C No	+5V	-5V
U301	10	5
U351	10	5

Fig. 7 Input Attenuator and Y-Amplifier Circuit Diagram

1425 MAIN BOARD, TIMEBASE & TRIGGER AND POWER SUPPLY (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
C710	10μF	E		25V	32180
C711	0.1μF	PE		1500V	40075
C712	0.1μF	PE		1500V	40075
C713	0.22μF	MF		100V	44370
C714	10nF	CE(3)		25V	450548
C715	0.22μF	MF		100V	44370
C716	10nF	CE(3)		25V	450548
C717	56pF	CE(3)			42417
C718	22pF	CE(3)			42412
C719	5.6nF	CE(2)			22394
C720	5.6pF	CE(3)			42405
C721		Capacitance Formed by Track Pattern			
C722	5.6nF	CE(2)			22394
C723	10nF	CE(3)		25V	450548
DIODES					
D201		Not Fitted			
D202		IN3595 or FD300			29330
D203	6V8	ZENER			33931
D231		Not Fitted			
D232		IN3595 or FD300			29330
D233	6V8	ZENER			33931
D301		SCHOTTKY			452035
D302		SCHOTTKY			452035
D303		IN4148			34701
D304		IN4148			34701
D351		SCHOTTKY			452035
D352		SCHOTTKY			452035
D353		IN4148			34701
D354		IN4148			34701
D401		IN4148			23802
D402		IN4148			23802
D403		IN4148			23802
D404	5V1	ZENER			33928
D405		IN4148			34701
D406		IN4148			34701
D501		IN4148			23802
D502		OA47			4468
D503		IN4148			23802
D504		IN4148			23802
D505		IN4148			23802
D506		IN4148			34701
D507		IN4148			23802
D508		IN4148			23802
D509		IN4148			23802
D510		IN4148			23802
D511		IN4148			23802
D512		IN4148			23802
D513		IN4148			23802
D514		IN4148			23802
D515		IN4148			23802
D516		IN4148			23802
D517		IN4148			23802
D518		IN4148			23802
D519		IN4148			23802
D520		IN4148			23802
D521	6V2	ZENER			33930
D522		IN4148			23802
D523		IN4148			23802
D524		SCHOTTKY			452035
D525		SCHOTTKY			452035
D601		IN4148			23802
D602		IN4148			23802
D603		IN4148			23802
D604		IN4148			23802
D605	5V6	ZENER			33929
D606		IN4148			23802
D607		IN4148			23802
D608		IN4148			23802
D609	47V	ZENER			40049
D610		IN4148			23802
D611		IN4148			23802
D701		IN4148			23802
D702		IN4148			23802
D704		L.E.D.			450922
D705		BAX17			402022
D706	150V	ZENER			37559
D708		IN4148			23802
D709	200V	ZENER			40052
D711	9V1	ZENER			33934
D712	5V1	ZENER			33928
D713		IN4148			23802
D714		IN4148			23802
D715	200V	ZENER			40052
D716	200V	ZENER			40052
D717	200V	ZENER			40052
D718	4Kv	E.H.T.			451803
D719	4Kv	E.H.T.			451803
D720		IN4148			23802
D721		BAX17			402022
D722		IN4004			450266
D723		IN4004			450266
D724		IN4004			450266
D725		IN4004			450266
D726		IN4004			450266
D727		IN4004			450266
D728		IN4004			450266
D729		IN4004			450266
D730	200V	ZENER			40052

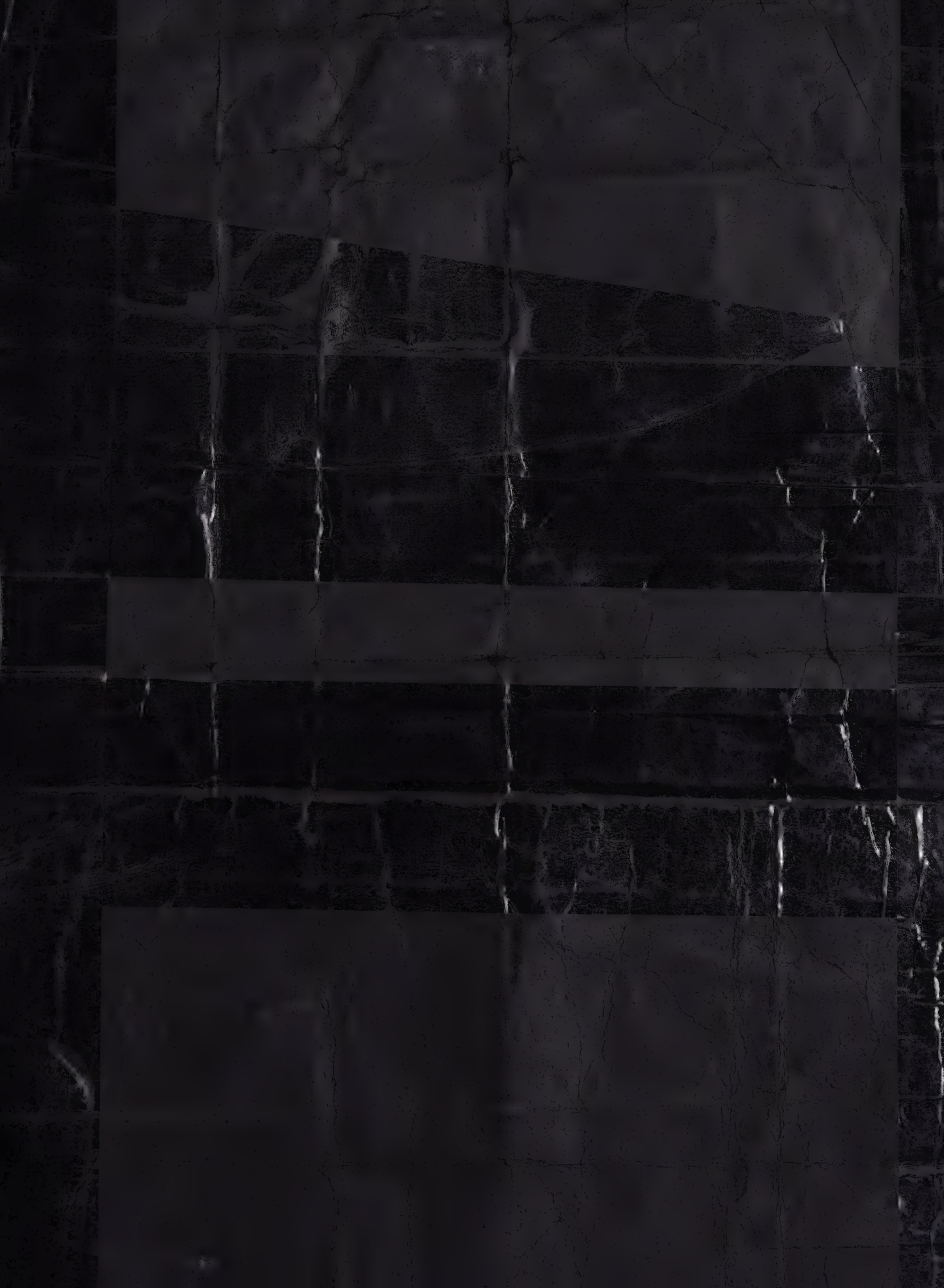
1425 MAIN BOARD, TIMEBASE & TRIGGER AND POWER SUPPLY (Cont.)

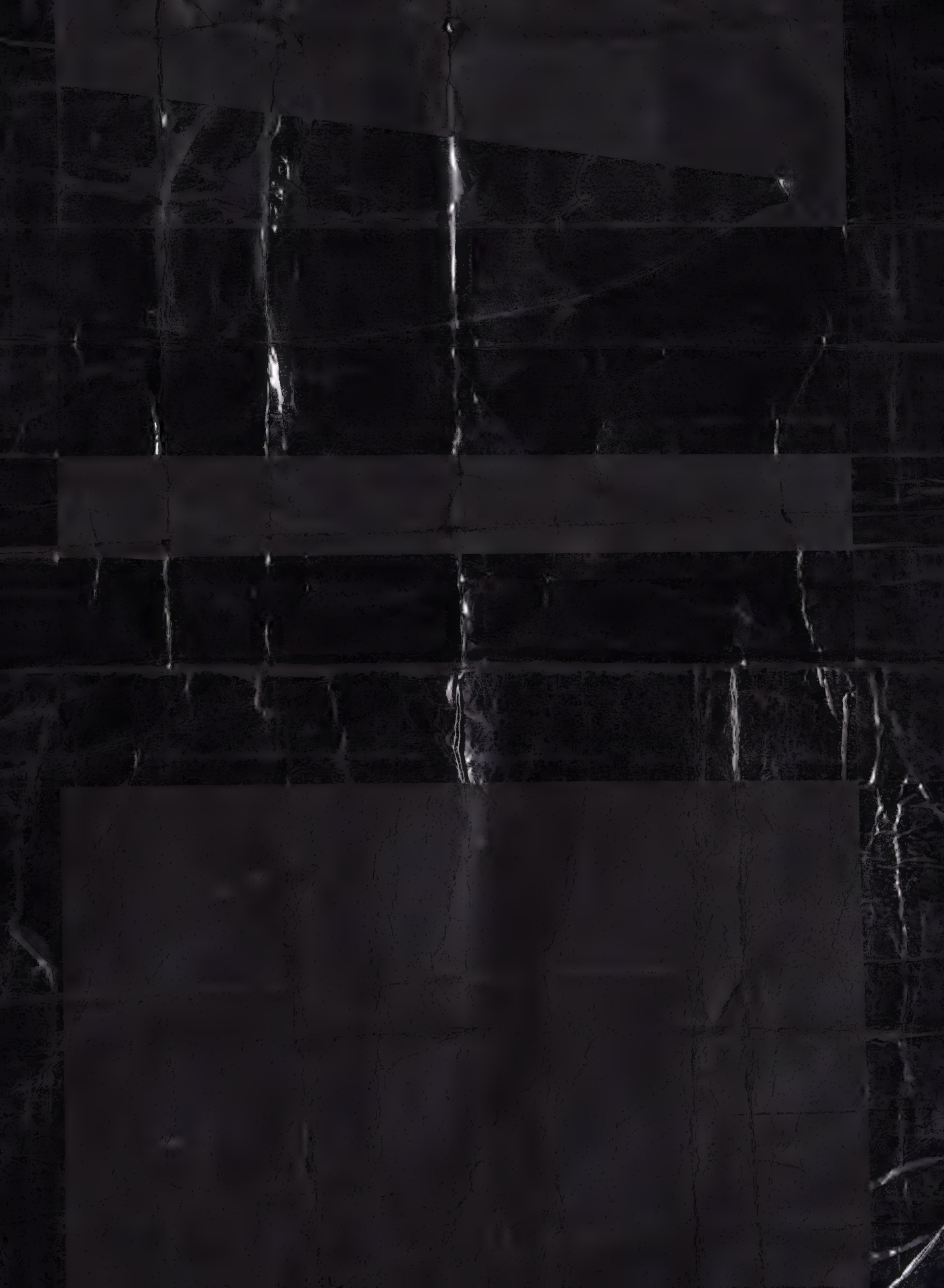
Ref	Value	Description	Tol %±	Rating	Part No
TRANSISTORS					
Q201		Dual Fet			452613
Q202					
Q203		CA3018			451797
Q204					
Q231		Dual Fet			452613
Q232					
Q233		CA3018			451797
Q234					
Q261		ZTX313			40788
Q262		BC547B			44951
Q263		BC558C			44952
Q264		BC558C			44952
Q401		BF371			36275
Q402		BF371			36275
Q403		BF371			36275
Q404		BF371			36275
Q405		ZTX313			40788
Q406		ZTX313			40788
Q407		BF468			40056
Q408		BF468			40056
Q501		BC547B			44951
Q502		MPS2369			36625
Q503		MPS2369			36625
Q504		BC547B			44951
Q505		2N3904			24146
Q506		BC558C			44952
Q507		BC557B			44950
Q508		BC557B			44950
Q509		BC547B			44951
Q511		2N3904			24146
Q512		2N3906			21533
Q513		NSD459			40054
Q514		NSD459			40054
Q515		BF393			450226
Q517		MPS2369			36625
Q518		MPS2369			36625
Q601		BC558C			44952
Q602		BC558C			44952
Q603		BC547B			44951
Q604		BC557B			44950
Q605		2N3904			24146
Q606		2N3904			24146
Q607		2N3906			21533
Q701		MPS2369			44953
Q702		BFR86B			44954
Q703		BFR86B			44954
Q704		BC558C			44952
Q706		BC548C			454432
Q707		BUX87			44955
Q709		BC328			38414
Q711		BC558C			44952
Q712		TIP112			40591
Q713		TIP112			40591
Q714		BC547B			44951
Q715		BC557B			44950
Q716		2N6518			36472
Q720		BC558C			44952
INTEGRATED CIRCUITS					
U261		LF351N			40130
U301		LM733CN			40084
U351		LM733CN			40084
U501		74LS74			36732
U552		VOL.REG.			40406
U601		MC3401P			40061
U602		IC710			40083
U701		VOL.REG.			40060
U702		LM341P15			40059
SWITCHES					
S1		(With R745)			453627
S2					4069
S3					4069
S101					453170
S102					452279
S131					453170
S201					454622
S231					454622
S261					44476
S262					453771
S301					38729
S501					38728
S502					38728
S503					38728
S504					38728
S505					38728
S506					38728
S507					38729

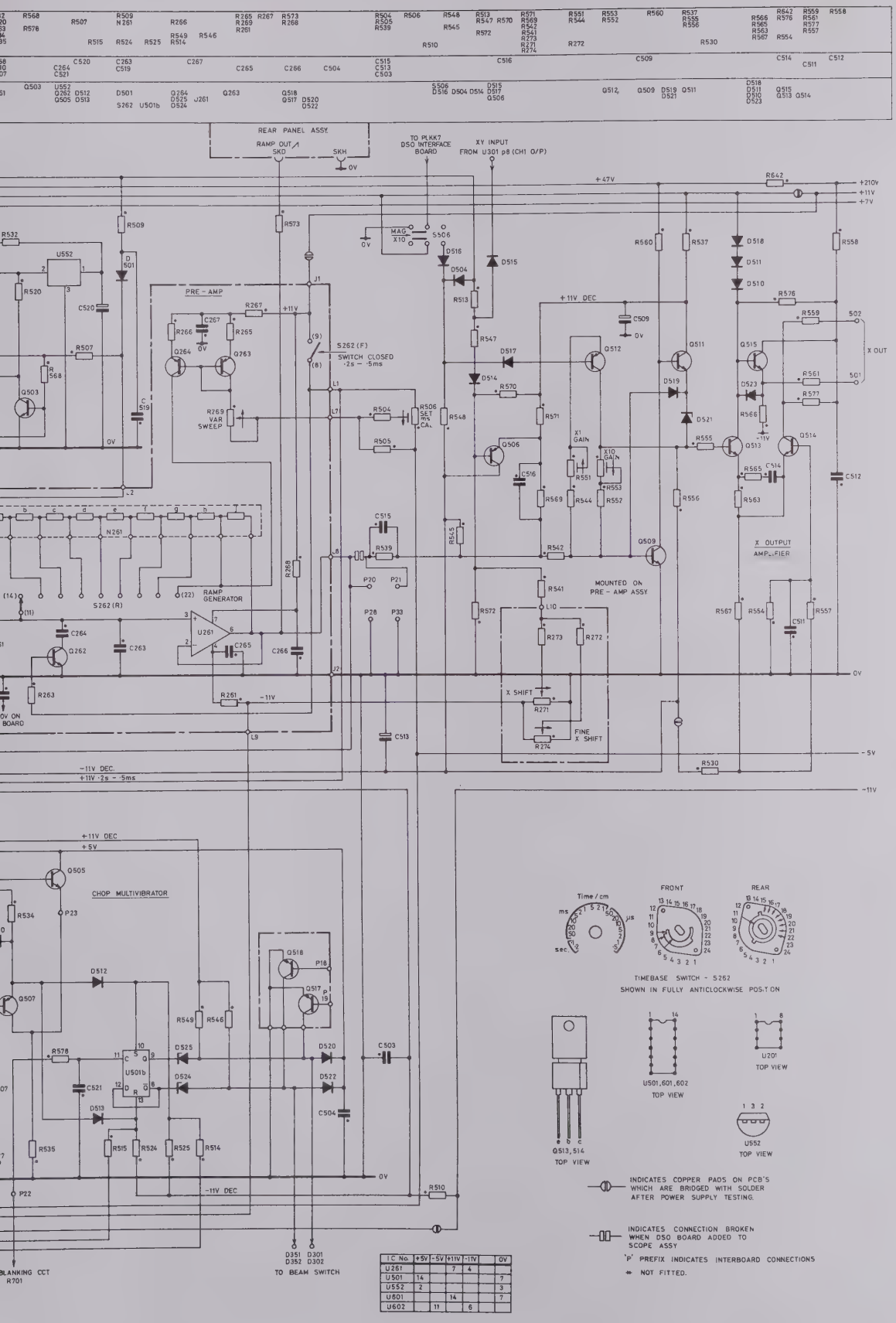
1425 MAIN BOARD, TIMEBASE & TRIGGER AND POWER SUPPLY (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
MISCELLANEOUS					
L1					44993
FS1	400mA for 240V Supply				454896
	800mA for 110V Supply				454897
FS701	125MA				450551
V1					452026
T1					453520
L401		Choke			44993
L402		Choke			44993

| | | |

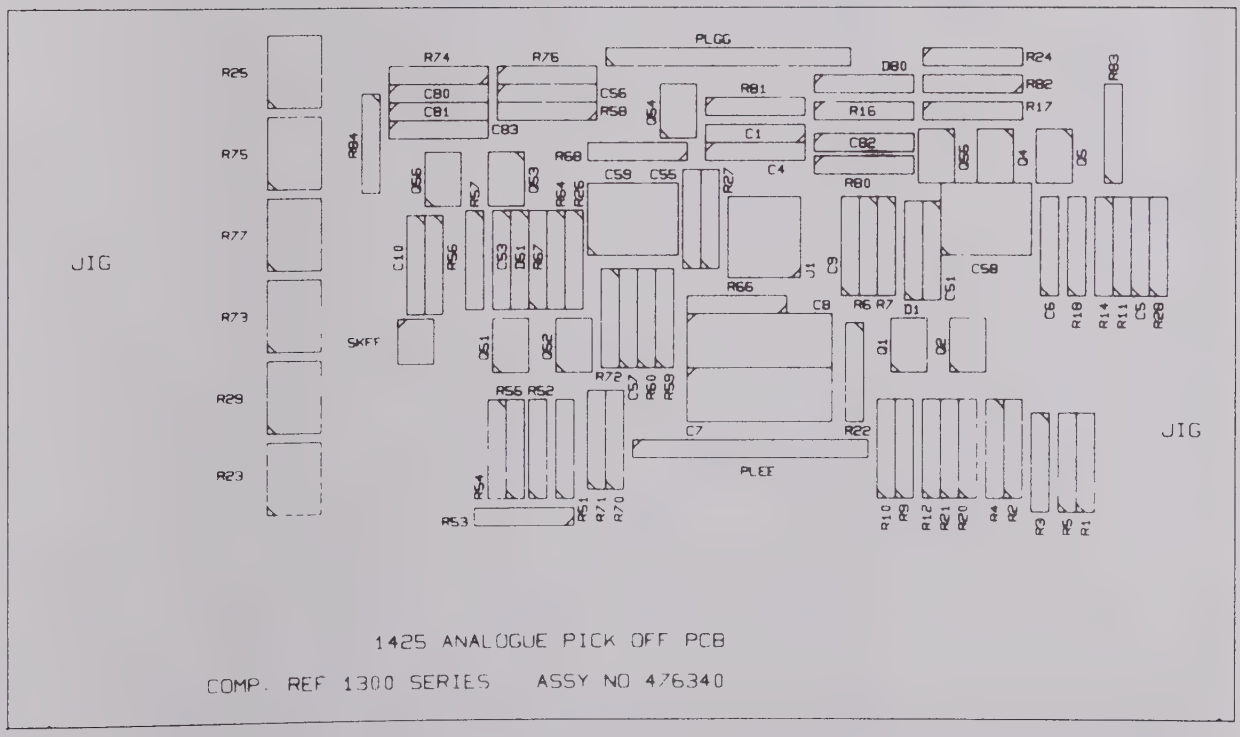






I C No.	+5V	-5V	+11V	-11V	0V
U261			7	4	
U501	14				7
U552	2				3
U601			14		7
U602		11		6	

Fig. 8 Timebase Circuit Diagram



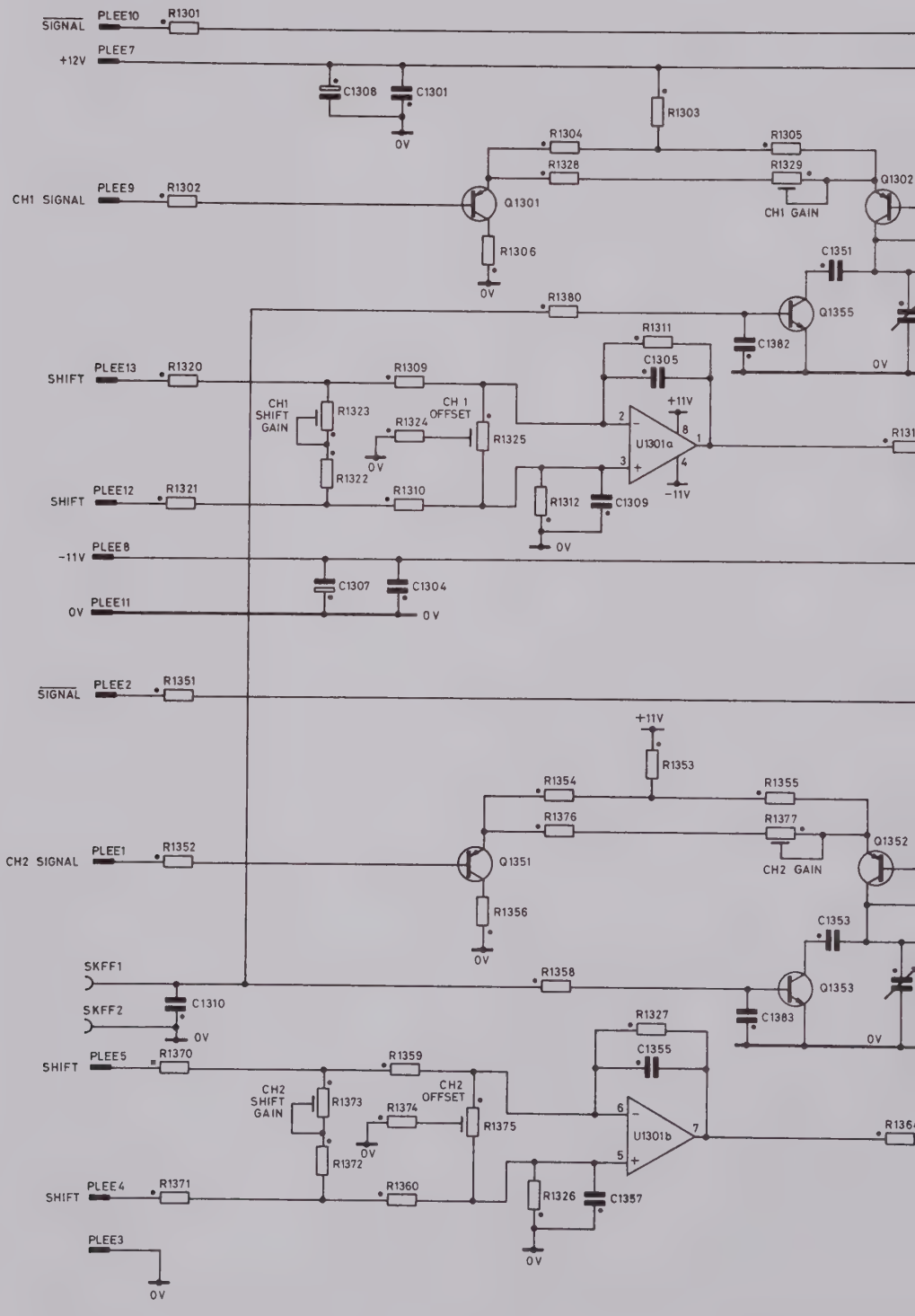
Pick-Off Printed Board

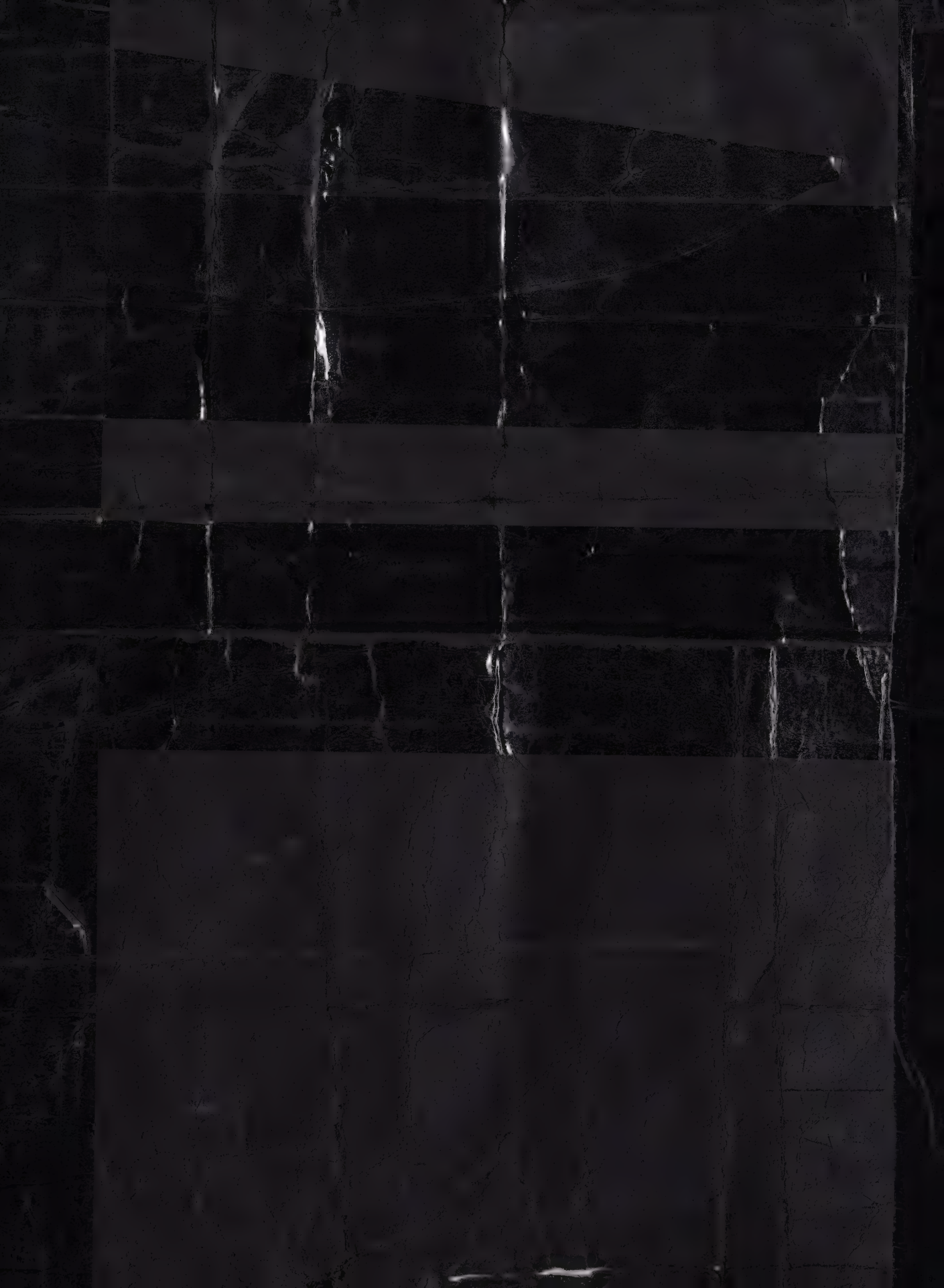
ANALOGUE PICKOFF 1425

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1301	47	CF			28714
R1302	47	CF			28714
R1303	560	CF			21798
R1304	220	CF			21796
R1305	220	CF			21796
R1306	270	CF			28720
R1307	220	CF			21796
R1309	15k	CF			28727
R1310	15k	CF			28727
R1311	100k	CF			21819
R1312	100k	CF			21819
R1314	1k5	CF			21801
R1316	560	MF	2		38588
R1317	47	CF			28714
R1318	220	CF			21796
R1320	18k	CF			21811
R1321	18k	CF			21811
R1322	22k	CF			21812
R1323	47k	PCP			42166
R1324	180k	CF			21822
R1325	100k	PCP			42167
R1326	100k	CF			21819
R1327	100k	CF			21819
R1328	470	CF			21797
R1329	1k	PCP			35898
R1351	47	CF			28714
R1352	47	CF			28714
R1353	560	CF			21798
R1354	220	CF			21796
R1355	220	CF			21796
R1356	270	CF			28720
R1357	220	CF			21796
R1358	4k7	CF			21805
R1359	15k	CF			28727
R1360	15k	CF			28727
R1364	1k5	CF			21801
R1366	560	MF	2		38588
R1367	47	CF			28714
R1368	220	CF			21796
R1370	18k	CF			21811
R1371	18k	CF			21811
R1372	22k	CF			21812
R1373	47k	PCP			42166
R1374	180k	CF			21822
R1375	100k	PCP			42167
R1376	470	CF			21797
R1377	1k	PCP			35898

Ref	Value	Description	Tol %±	Rating	Part No
R1380	4k7	CF			21805
R1381	2k2	MF	2		38602
R1382	560	MF	2		38588
R1383	68	CF			28716
R1384	68	CF			28716
CAPACITORS					
C1301	10nF	CE(3)		25V	450548
C1304	10nF	CE(3)		25V	450548
C1305	100nF	CE(3)			43498
C1306	10nF	CE(3)		25V	450548
C1307	10µF	E		25V	32180
C1308	10µF	E		25V	32180
C1309	100nF	CE(3)			43498
C1310	10nF	CE(3)		25V	450548
C1351	270pF	CE(3)			42425
C1353	270pF	CE(3)			42425
C1355	100nF	CE(3)			43498
C1356	10nF	CE(3)		25V	450548
C1357	100nF	CE(3)			43498
C1358		Trimmer			43503
C1359		Trimmer			43503
C1380	10nF	CE(3)		25V	450548
C1381	100nF	CE(3)			43498
C1382	100nF	CE(3)			43498
C1383	100nF	CE(3)			43498
DIODES					
D1301		IN4148			23802
D1351		IN4148			23802
D1380		IN4148			23802
TRANSISTORS					
Q1301		ZTX510			453174
Q1302		ZTX510			453174
Q1304		MPS2369			36625
Q1305		2N3904			24146
Q1351		ZTX510			453174
Q1352		ZTX510			453174
Q1353		BF371			36275
Q1354		MPS2369			36625
Q1355		BF371			36275
Q1356		2N3904			24146
INTEGRATED CIRCUITS					
U1301		TLO82CP			451262

RES.	R1301 R1302 R1320 R1321 R1351 R1352 R1370 R1371	R1323 R1322 R1373 R1372	R1309 R1324 R1310 R1359 R1374 R1360	R1306 R1325 R1356 R1375	R1304 R1328 R1380 R1312 R1354 R1376 R1358 R1326	R1303 R1311 R1353 R1327	R1305 R1329 R1355 R1377		R131 R136
CAPS.	C1310	C1308 C1307	C1301 C1304		C1309 C1357	C1305 C1355	C1382 C1383	C1351 C1353	
MISC.				Q1301 Q1351		U1301a,b	Q1355 Q1353		Q1302 Q1352





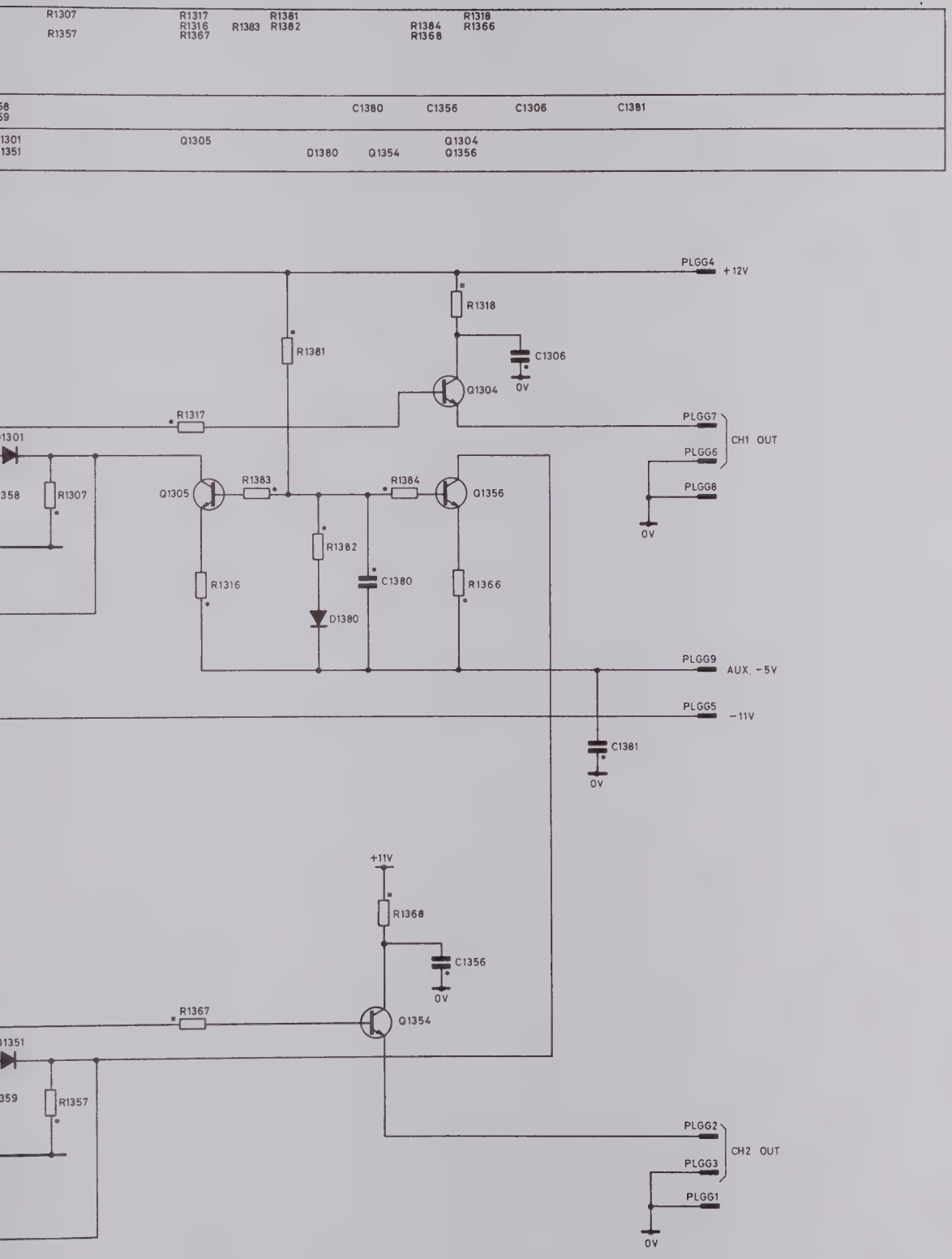
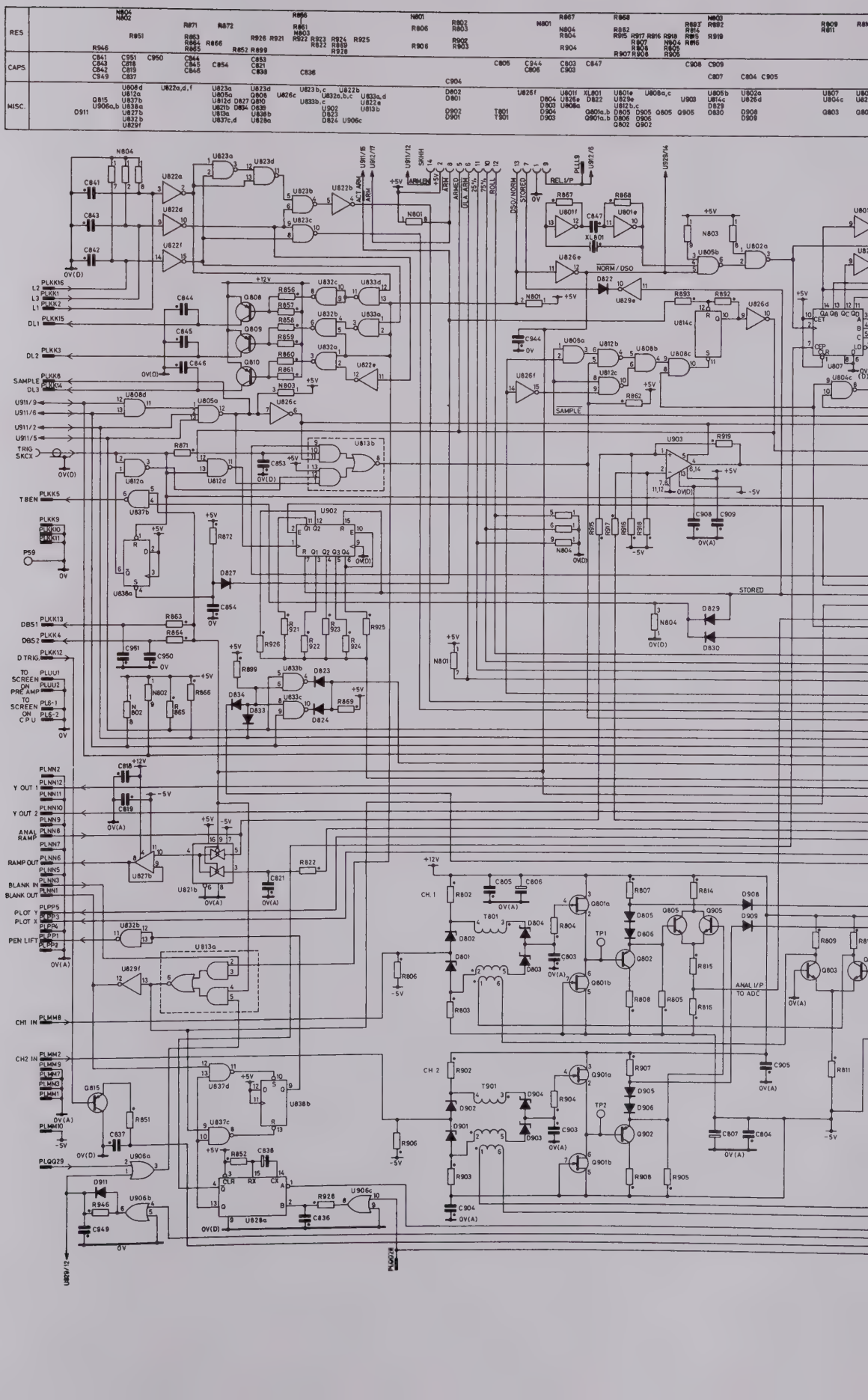
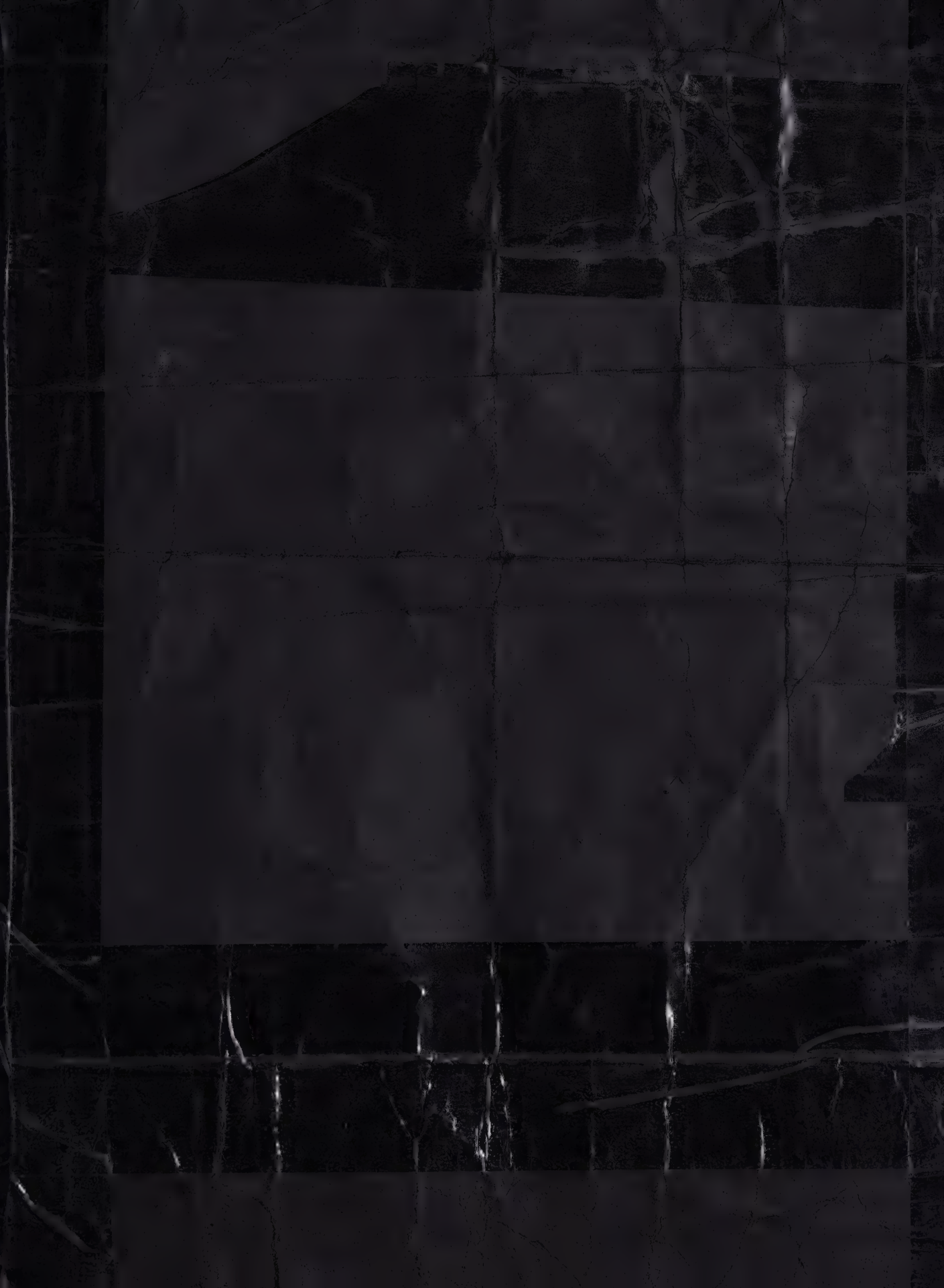


Fig. 9 Analogue Pick-Off Circuit Diagram

DSO 1425

	Ref	Value	Description	Tol %±	Rating	Part No	Ref	Value	Description	Tol %±	Rating	Part No
	RESISTORS											
F9	R802	10k	CF			21809	R858	22k	CF			21812
G9	R803	2k2	CF			21802	R859	22k	CF			21812
F8	R804	47	CF			28714	R860	5k6	CF			21806
F8	R805	5k6	CF			21806	R861	22k	CF			21812
G10	R806	330	CF			28721	R862	4k7	CF			21805
F8	R807	1k8	CF			28725	R863	15k	CF			2872
G8	R808	100	CF			21794	R864	15k	CF			2872
G10	R809	470	CF			21797	R865	4k7	CF			21805
G10	R810	470	CG			21797	R866	4k7	CF			21805
G10	R811	130	MF	2		38573	R867	680	CF			2872
G7	R812	390	CF			28722	R868	680	CF			28723
							R869	18k	CF			21811
F8	R814	100	CF			21794						
F8	R815	47	CF			28714	R871	330	CF			2872
G8	R816	820	CF			28724	R872	47k	CF			2181
F10	R817	5k6	CF			21806						
G7	R818	680	CF			28723	R874	47k	CF			2181
G7	R819	3k9	CF			21804						
K10	R820	6k8	CF			21807	R880	100	CF			2179
L10	R821	10k	PCP			36267	R881	16k	MF	2		3862
J10	R822	180	CF			21795	R882	16k	MF	2		3862
K10	R823	3k	MF	2		38605	R883	7k5	MF	2		3861
K10	R824	3k	MF	2		38605	R884	7k5	MF	2		3861
K10	R825	3k9	CF			21804	R885	560	CF			2179
K10	R826	3k9	CF			21804	R886	6k2	MF	2		3861
K10	R827	5k6	CF			21806	R887	6k2	MF	2		3861
K10	R828	5k6	CF			21806						
J10	R829	1k	PCP			36264	R891	10k	CF			2180
K10	R830	220	MF	2		38578	R892	180k	CF			2182
L9	R831	220	MF	2		38578	R893	33k	CF			2181
H10	R832	100	CF			21794						
J9	R833	820	CF			28724	R896	150	CF			2871
G9	R834	470	PCP			36263						
G9	R835	1k5	CF			21801	R899	10k	CF			2180
H8	R836	1k5	CF			21801						
J9	R837	18k	CF			21811	R902	10k	CF			2180
H9	R838	10k	PCP			36267	R903	2k2	CF			2180
J9	R839	18k	CF			21811	R904	47	CF			2871
H9	R840	560	CF			21798	R905	5k6	CF			2180
H8	R841	5k6	CF			21806	R906	330	CF			2872
H7	R842	220	PCP			36262	R907	1k8	CF			2872
H8	R843	390	MF	5		28722	R908	100	CF			2179
J8	R844	6k2	MF	2		38613	R909	470	CF			2179
J8	R845	6k2	MF	2		38613	R910	470	CF			2179
H8	R846	6k2	MF	2		38613	R911	130	MF	2		3851
G8	R847	620	MF	2		38589	R912	470	CF			2179
K5	R848	18k	CF			21811	R913	120	MF	2		3857
H8	R849	22k	CF			21812						
E5	R850	100k	CF			21819	R915	120	MF	2		3857
F2	R851	330k	CF			28721	R916	1k2	MF	2		3859
G2	R852	100k	CF			21819	R917	120	MF	2		3857
E5	R853	18k	CF			21811	R918	1k2	MF	2		3859
E4	R854	10k	CF			21809	R919	33k	CF			2181
J8	R855	6k2	MF	2		38613	R920	4k7	CF			2180
G2	R856	22k	CF			21812	R921	330k	CF			3235
G1	R857	22k	CF			21812	R922	5M6	CF	10		33260


RES
CAPS
MISC.
ARMED
ARM
STORED
NORM / DSO
SAMPLE
TRIG SKCK
TBEN
DBS1
DBS2
D TRIG.
Y OUT 1
Y OUT 2
ANAL RAMP
RAMP OUT
BLANK IN
BLANK OUT
PLOT Y
PLOT X
PEN LIFT
CH1 IN
CH2 IN
CH. 1
CH. 2
ANAL U/P TO ADC
TO SCREEN ON PRE AMP
TO SCREEN ON C P U



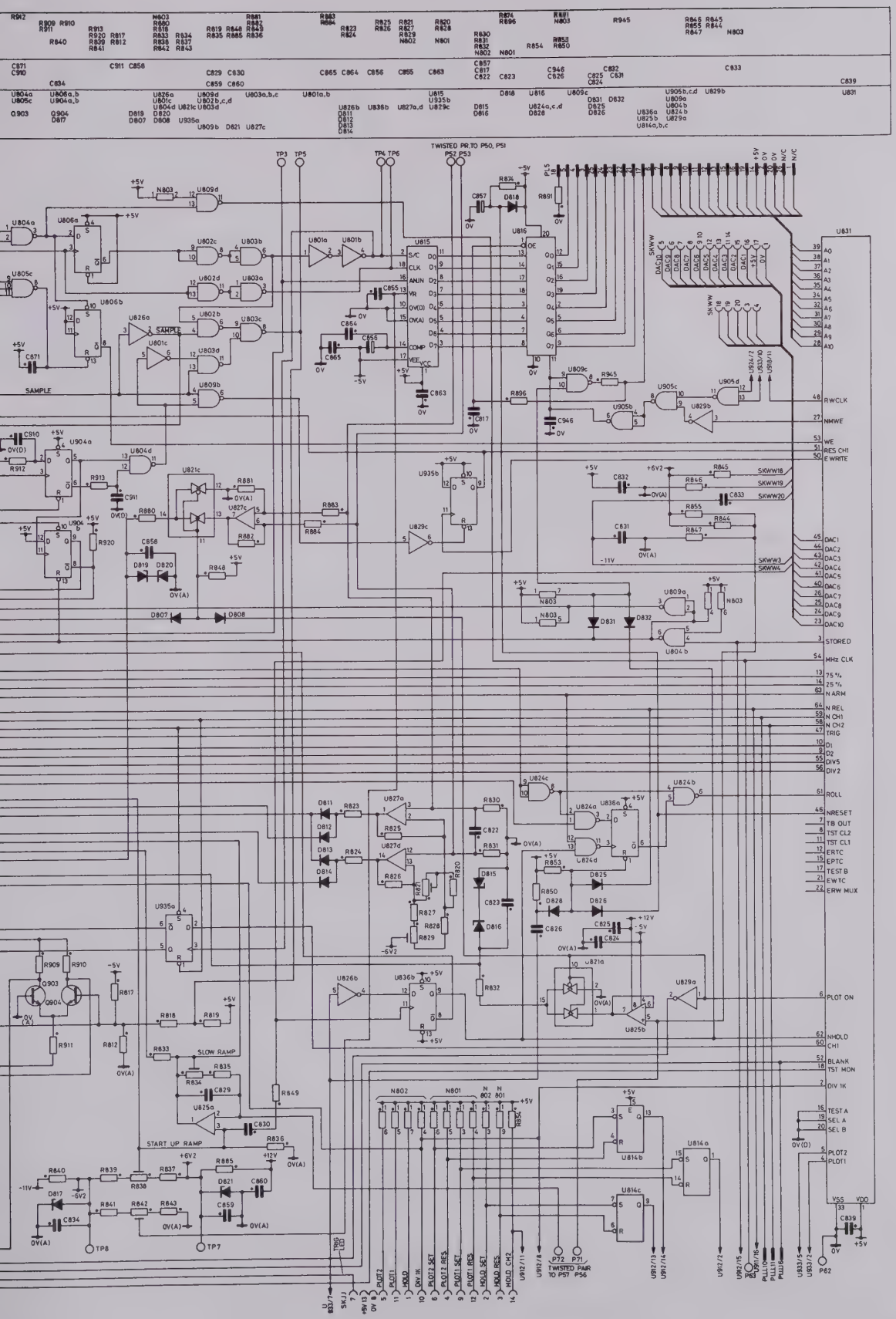


Fig. 10A Digital Storage Board Circuit Diagram

DSO 1425 (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
J8	R923	2M7	CF	10		30758
J7	R924	1M5	CF	10		40729
J7	R925	680k	CF			31839
J8	R926	150k	CF			21821
H1	R928	680	CF			28723
B9	R931	47k	CF			21815
B3	R932	47k	CF			21815
B9	R933	82k	CF			21818
B8	R934	56k	CF			28729
B9	R935	10	CF			21793
A9	R936	100	CF			21794
B9	R937	22k	CF			21812
B9	R938	10k	CF			21809
B9	R939	10	CF			21793
A8	R940	10k	CF			21809
B8	R941	56k	CF			28729
C5	R942	47k	CF			21815
B7	R943	47k	CF			21815
D3	R944	560	CF			21798
L5	R945	47	CF			28714
H1	R946	4k7	CF			21805
E5	N801	10k x 8	Resistor Network			450452
E4	N802	10k x 8	Resistor Network			450452
K3	N803	4k7 x 8	Resistor Network			39225
F4	N804	10k x 8	Resistor Network			450452
C10	N811	47k x 8	Resistor Network			450602
C10	N812	47k x 8	Resistor Network			450602
B8	N813	47k x 8	Resistor Network			450602
B5	N814	47k x 5	Resistor Network			453652
	CAPACITORS					
G9	C803	220pF	PS		63V	35914
F10	C804	10nF	CE(3)		25V	450548
E8	C805	10nF	CE(3)		25V	450548
F7	C806	10µF	E		25V	32180
F10	C807	10µF	E		25V	32180
H10	C809	10µF	E		25V	32180
G10	C810	10µF	E		25V	32180
H10	C811	10nF	CE(3)		25V	450548
H11	C812	10µF	E		25V	32180
H10	C813	10nF	CE(3)		25V	450548
J11	C814	10µF	E		25V	32180
J10	C815	10nF	CE(3)		25V	450548
K10	C816	10nF	CE(3)		25V	450548
G5	C817	120pF	CE(3)			42421
K9	C818	10nF	CE(3)		25V	450548
K10	C819	10nF	CE(3)		25V	450548
J9	C821	1nF	CE(3)			42432
K9	C822	2.2nF	CE(3)			42436
H10	C823	100nF	CE(3)			43498

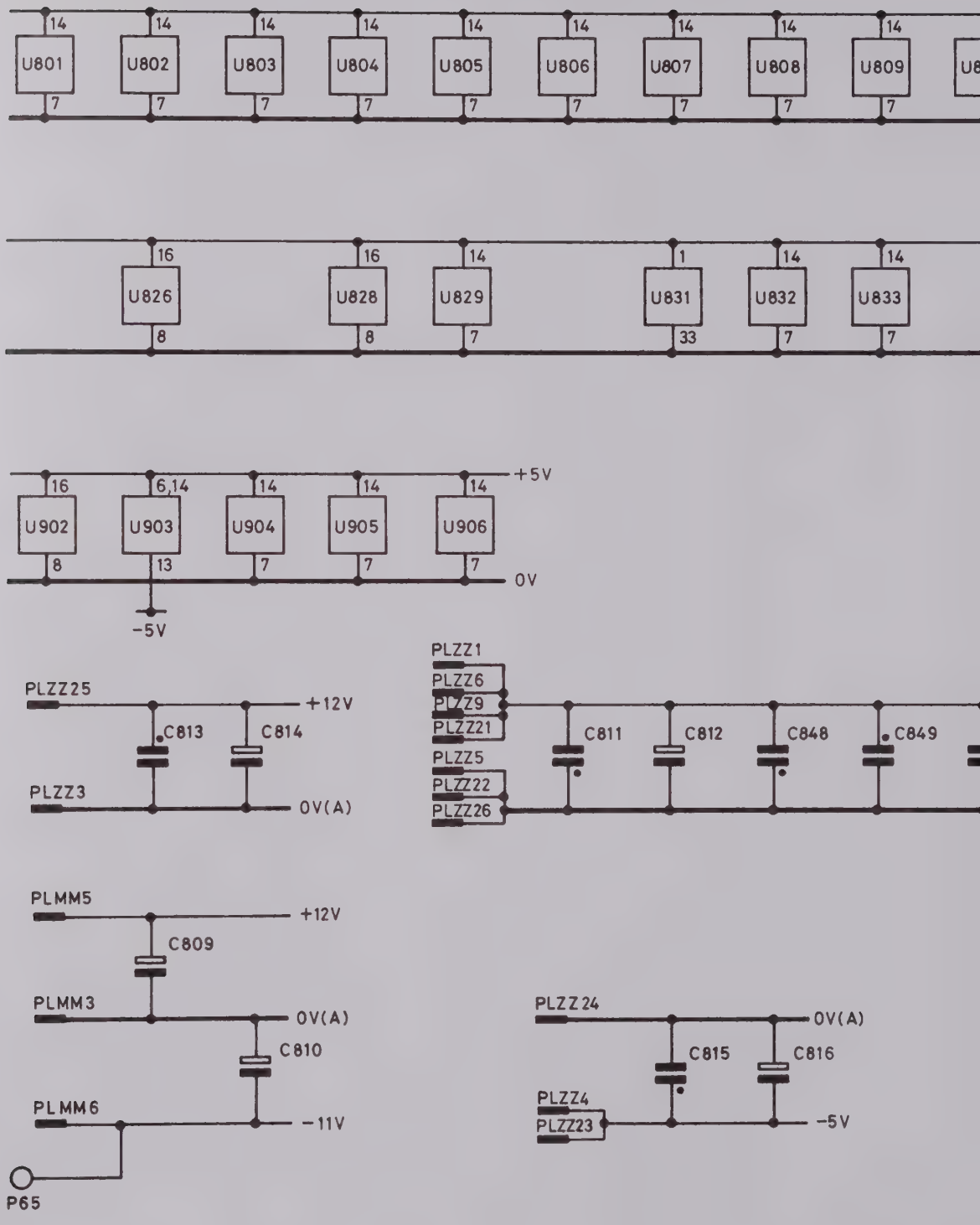
Ref	Value	Description	Tol %±	Rating	Part No
C824	10nF	CE(3)		25V	450548
C825	10nF	CE(3)		25V	450548
C826	1nF	CE(3)			42432
C829	100pF	CE(3)			42420
C830	5.6pF	CE(3)			42405
C831	100nF	CE(3)			43498
C832	100nF	CE(3)			43498
C833	10nF	CE(3)		25V	450548
C834	100nF	CE(3)			43498
C836	10nF	CE(3)		25V	450548
C837	100nF	CE(3)			43498
C838	10µF	E		25V	32180
C839	10nF	CE(3)		25V	450548
C841	100nF	CE(3)			43498
C842	100nF	CE(3)			43498
C843	100nF	CE(3)			43498
C844	100nF	CE(3)			43498
C845	100nF	CE(3)			43498
C846	100nF	CE(3)			43498
C847	47pF	CE(3)			42416
C848	10nF	CE(3)		25V	450548
C849	10nF	CE(3)		25V	450548
C850	10nF	CE(3)		25V	450548
C851	10nF	CE(3)		25V	450548
C852	10nF	CE(3)		25V	450548
C853	3.3nF	CE(3)		50V	42438
C854	47nF	CE(3)			43497
C855	100nF	CE(3)			43498
C856	2.2µF	E		63V	32194
C857	10µF	E		25V	32180
C858	100nF	CE(3)			43498
C859	10nF	CE(3)		25V	450548
C860	100nF	CE(3)			43498
C861	10nF	CE(3)		25V	450548
C862	100nF	CE(3)			43498
C863	10nF	CE(3)		25V	450548
C864	1nF	CE(3)			42432
C865	10nF	CE(3)		25V	450548
C868	10nF	CE(3)		25V	450548
C869	10nF	CE(3)		25V	450548
C870	10nF	CE(3)		25V	450548
C871	18pF	CE(3)	10		42411
C903	220pF	PS		63V	35914
C904	10nF	CE(3)		25V	450548
C905	10nF	CE(3)		25V	450548
C908	10nF	CE(3)		25V	450548
C909	10nF	CE(3)		25V	450548
C910	47nF	CE(3)			43497
C911	220pF	CE(3)			42424
C921	10nF	CE(3)		25V	450548

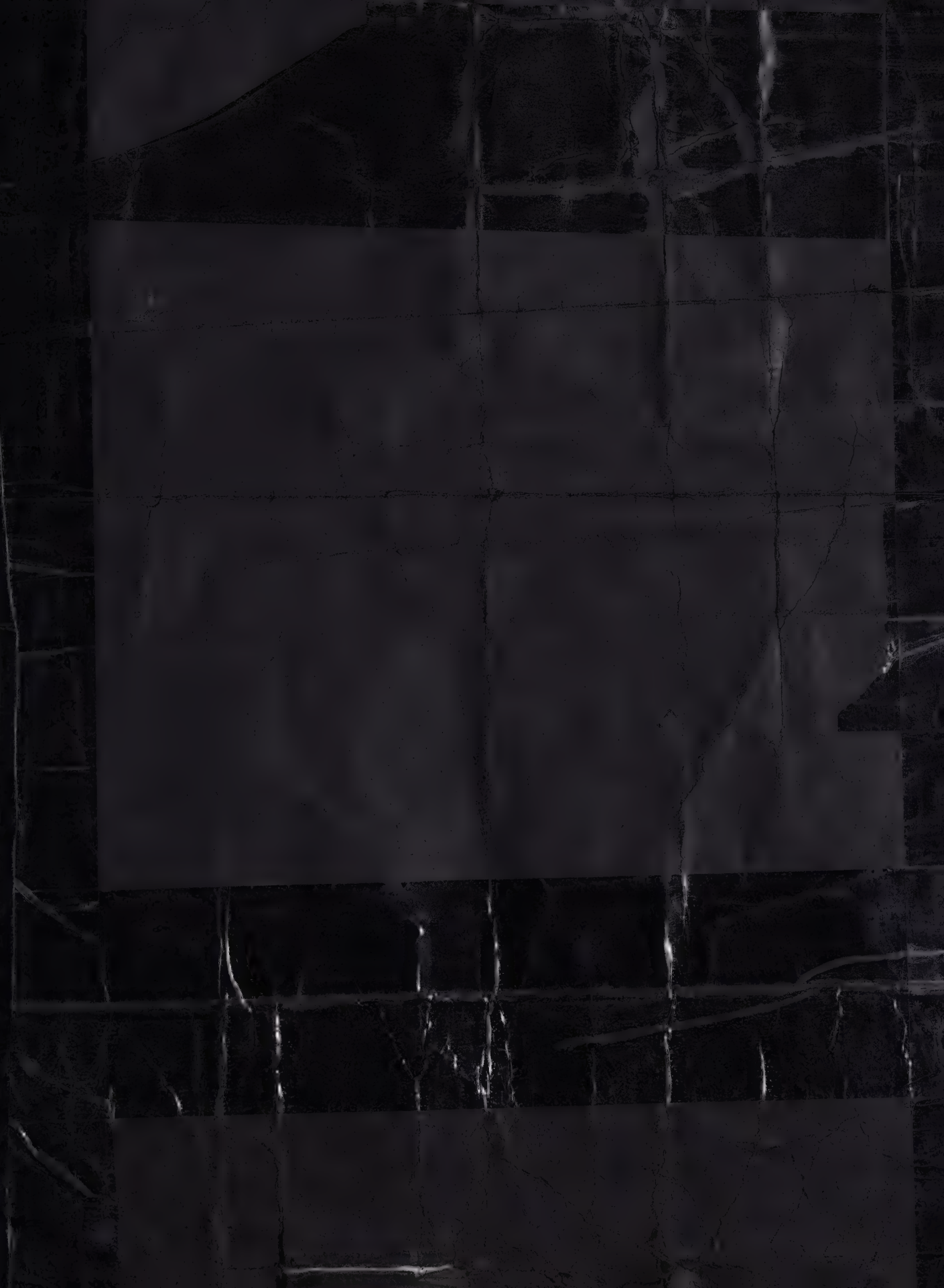
DSO 1425 (Cont.)

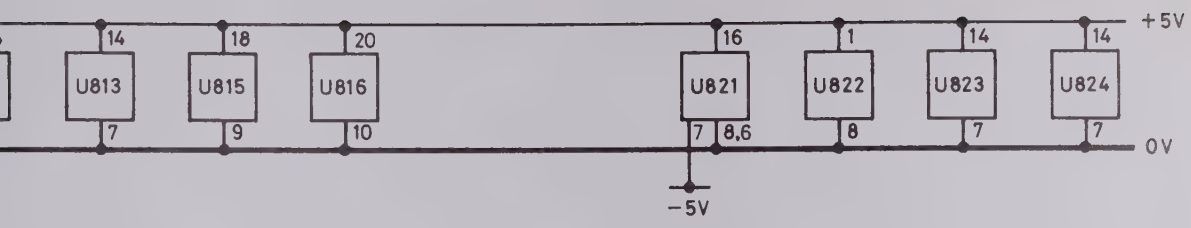
Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
A9	C923	220pF	E	16V	32176
B9	C924	82pF	CE(3)		42419
B9	C925	22nF	MF	100V	39191
A9	C926	220pF	CE(3)		43499
B8	C930	4.7µF	E	63V	32195
N10	C931	220µF	E	25V	32184
D8	C932	10nF	CE(3)	25V	450548
B7	C933	10nF	CE(3)	25V	450548
C10	C934	10nF	CE(3)	25V	450548
B4	C935	10nF	CE(3)	25V	450548
B2	C936	10nF	CE(3)	25V	450548
C5	C937	10nF	CE(3)	25V	450548
C4	C938	10nF	CE(3)	25V	450548
C2	C939	10nF	CE(3)	25V	450548
C9	C940	10nF	CE(3)	25V	450548
C7	C941	10nF	CE(3)	25V	450548
D4	C942	22µF	T	35V	35932
D3	C943	10nF	CE(3)	25V	450548
F7	C944	10nF	CE(3)	25V	450548
D2	C945	100nF	CE(3)		43498
K3	C946	68pF	CE(3)		42418
G1	C949	3.3nF	CE(3)		42438
E9	C950	100nF	CE(3)		43498
E9	C951	100nF	CE(3)		43498
L4	C952	10nF	CE(3)	25V	450548
DIODES					
G10	D801	2V7	ZENER		33921
G10	D802	2V7	ZENER		33921
F9	D803		SCHOTTKY		32671
G9	D804		SCHOTTKY		32671
F8	D805		IN4148		23802
F8	D806		IN4148		23802
K5	D807		OA47		4468
K5	D808		OA47		4468
K10	D811		IN4148		23802
K10	D812		IN4148		23802
K10	D813		IN4148		23802
K10	D814		IN4148		23802
H10	D815	3V9	ZENER		33925
H10	D816	3V9	ZENER		33925
H9	D817		IN823		40045
L5	D818		IN4148		23802
J10	D819	3V9	ZENER		33925
J10	D820	3V9	ZENER		33925
J8	D821		IN823		40045
J5	D822		IN4148		23802
G3	D823		OA47		4468
G3	D824		OA47		4468
E5	D825		OA47		4468
D5	D826		OA47		4468
D7	D827		OA47		4468
E5	D828		OA47		4468
D829			OA47		4468 J5
D830			OA47		4468 E7
D831			OA47		4468 K4
D832			OA47		4468 L4
D833			IN4148		23802 G3
D834			IN4148		23802 F4
D901	2V7		ZENER		33921 F10
D902	2V7		ZENER		33921 E10
D903			SCHOTTKY		32671 E9
D904			SCHOTTKY		32671 F9
D905			IN4148		23802 E8
D906			IN4148		23802 E8
D908			IN4148		23802 F8
D909			IN4148		23802 F8
D910			IN823		40045 D2
D911			IN4148		23802 H1
TRANSISTORS					
Q801			U412		452613 G8
Q802			ZTX510		453174 G8
Q803			MPS2369		36625 G10
Q804			MPS2369		36625 G10
Q805			MPS2369		36625 F8
Q808			2N3906		21533 F1
Q809			2N3906		21533 F2
Q810			2N3906		21533 F1
Q815			2N3906		21533 F2
Q901			U412		452613 E8
Q902			ZTX510		453174 E8
Q903			MPS2369		36625 E10
Q904			MPS2369		36625 E10
Q905			MPS2369		36625 F8
Q911			2N3904		24146 B9
U801			74ALS04		451301 J3
U802			74ALS00		451299 H3
U803			74ALS00		451299 H3
U804			74LS00		36730 J4
U805			74LS10		36867 J4
U806			74ALS74		451308 H4
U807			74ALS162		451313 H4
U808			4081		36794 G4
U809			74ALS00		451299 L5
U812			4011		34593 G3
U813			74L551		43676 L6
U814			4044		44024 F6
U815			TDC1001J		450682 G7
U816			74LS374		43386 G6

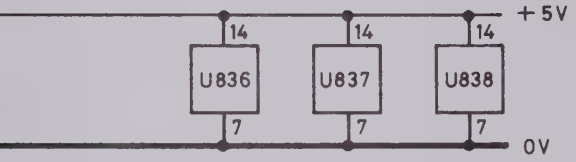
DSO 1425 (Cont.)

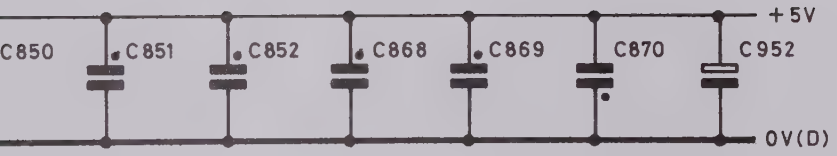
Ref	Value	Description	Tol %±	Rating	Part No
TRANSISTORS (Cont.)					
D3	U820	DAC-08AH			450686
J9	U821	4053			41891
F4	U822	4049			36200
F3	U823	4011			34593
C1	U824	74C00			451282
H9	U825	TL082CP			451262
F7	U826	4049			36200
K9	U827	LF347N			450908
H2	U828	74LS123			41084
J5	U829	74ALS04			451301
J5	U831	MT70009			450600
F3	U832	74LS26			44362
F4	U833	4011			34953
C2	U836	74C74			451290
D1	U837	74C00			451282
D2	U838	74C74			451290
K8	U902	4520			450914
L8	U903	NE521			44886
K5	U904	74ALS74			451308
L4	U905	74LS00			34730
H1	U906	74HC32			452265
C9	U911	74C374			451266
B3	U912	74C244			450913
B10	U913	4503			41295
C10	U914	74C244			450913
C6	U916	74ALS245			451953
C3	U917	74C374			451266
C3	U918	74C374			451266
U919		MB8128-15 or MBM8128-15			450683
U921		KEYPAD Option only			
U922		4503			41295
U923		74C374			451266
U924		74LS367			47051
U925		74C173			452560
U926		4503			41295
U927		74HC173			452972
U928		74HC374			451728
U929		4503			41295
U930		4503			41295
U931		DAC10GX 10 BIT			451264
U932		74HC00			451956
U933		40174/74C174			37057
U935		74ALS74			451308
MISCELLANEOUS					
XL801		20MHz			450688
T801					450687
T901					450687
SKCX					36105
SKHH		14-way DIL			450771
SKJJ		14-way DIL			450771
PL5		26-way CABLE			453950


U801
U802
U803
U804
U805
U806
U807
U808
U809
U826
U828
U829
U831
U832
U833
U902
U903
U904
U905
U906
+5V
0V
-5V
PLZZ25
+12V
C813
C814
PLZZ3
0V(A)
PLZZ1
PLZZ6
PLZZ9
PLZZ21
C811
C812
C848
C849
PLZZ5
PLZZ22
PLZZ26
PLMM5
+12V
C809
PLMM3
0V(A)
C810
PLMM6
-11V
P65
PLZZ24
0V(A)
C815
C816
PLZZ4
PLZZ23
-5V









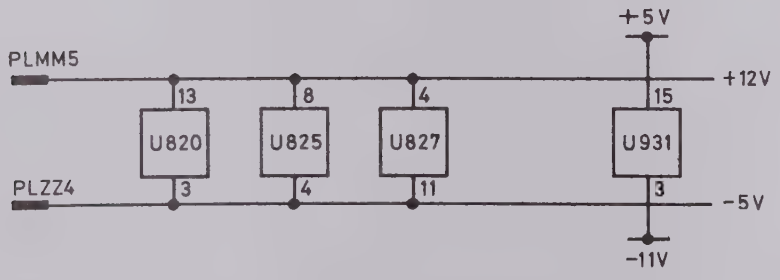


Fig 10B D.S.O. Power Connections Circuit Diagram

FOR COMPONENTS LIST SEE PAGES
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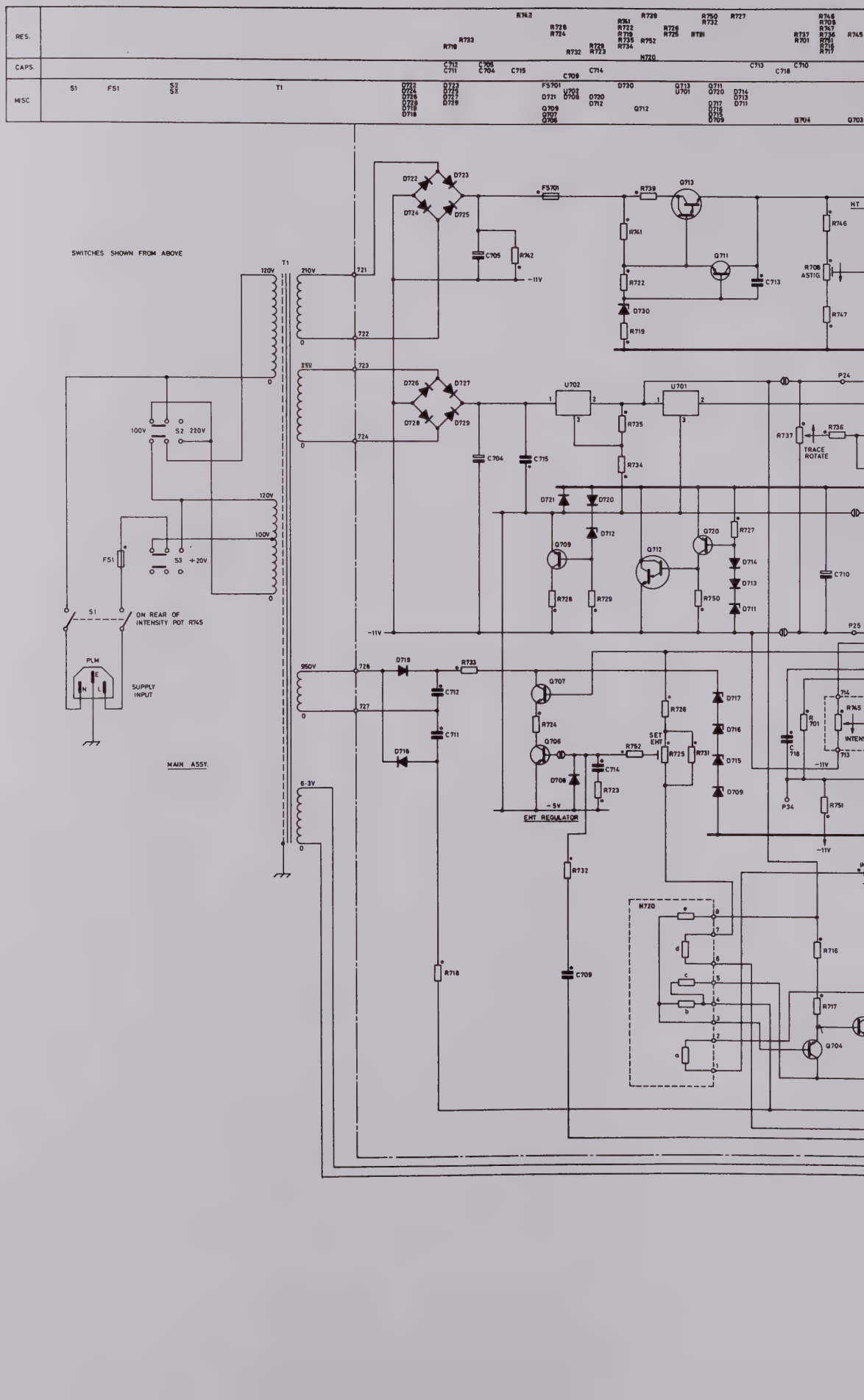
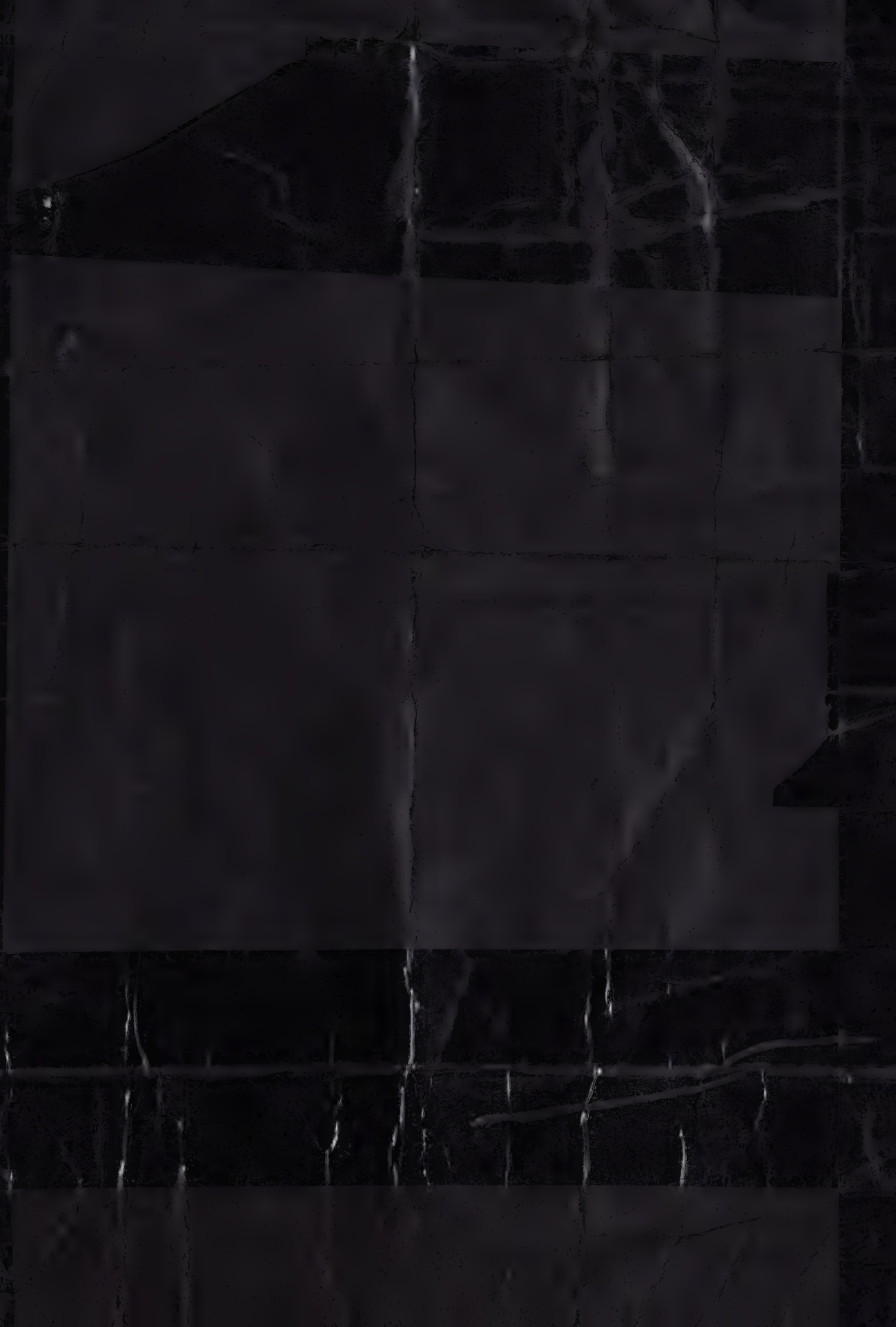

RES.
CAPS.
MISC
SWITCHES SHOWN FROM ABOVE
T1
120V
210V
0
721
722
S1
FS1
S2
S3
100V
220V
+20V
ON REAR OF INTENSITY POT R745
PLM
SUPPLY INPUT
MAIN ASSY.
D722
D723
D724
D725
FS701
R739
Q713
HT
R746
R761
Q711
R722
C713
R708 ASTIG.
D730
R719
R747
723
724
D726
D727
D728
D729
U702
U701
P24
R735
R734
C704
C715
R737
R736
TRACE ROTATE
D721
D720
D712
Q709
Q712
Q720
R727
D714
D713
D711
R728
R729
R750
C710
-11V
P25
950V
726
727
D719
R733
C712
C711
D718
Q707
R724
Q706
R726
SET EHT
R725
R731
R752
C714
D708
R723
-5V
EHT REGULATOR
D717
D716
D715
D709
R745
R701
C718
P34
R751
6·3V
R732
R718
C709
M720
R716
R717
Q704



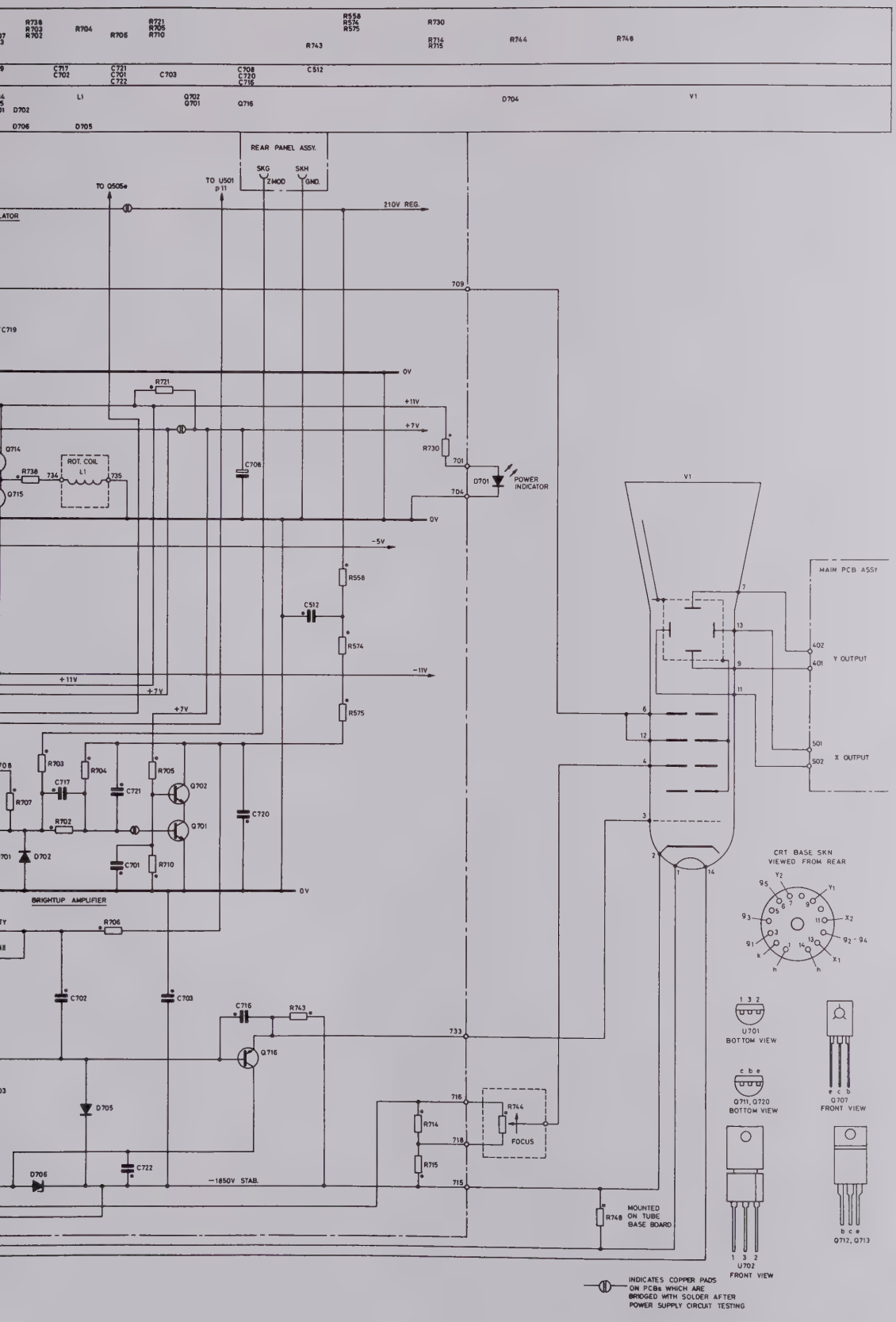
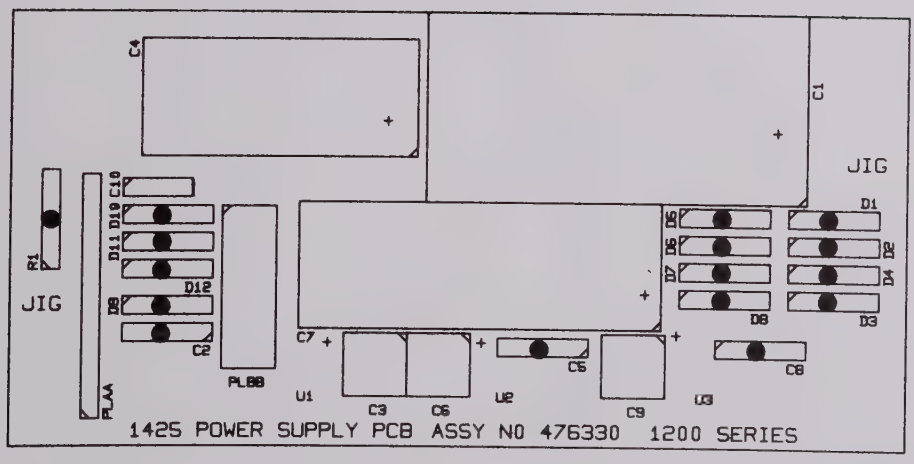


Fig. 11 Main Power Supply Circuit Diagram

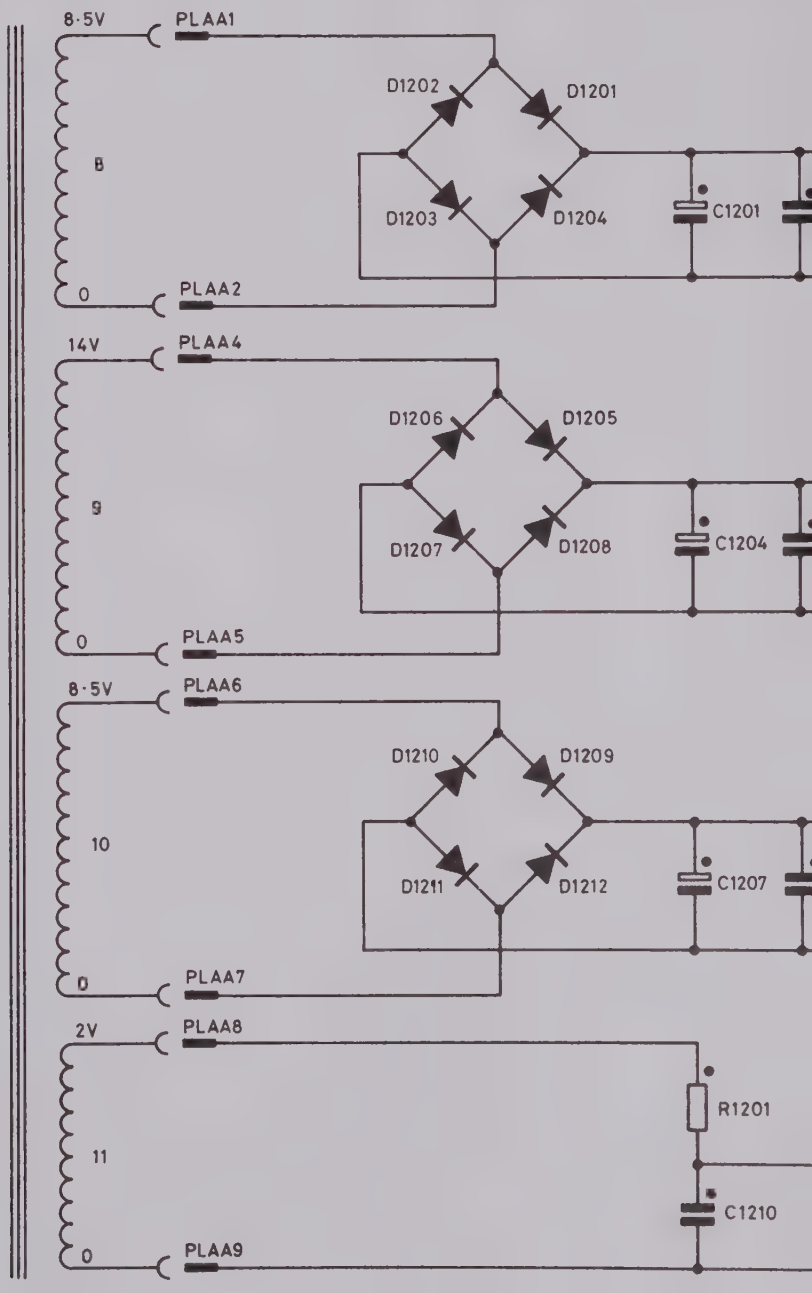


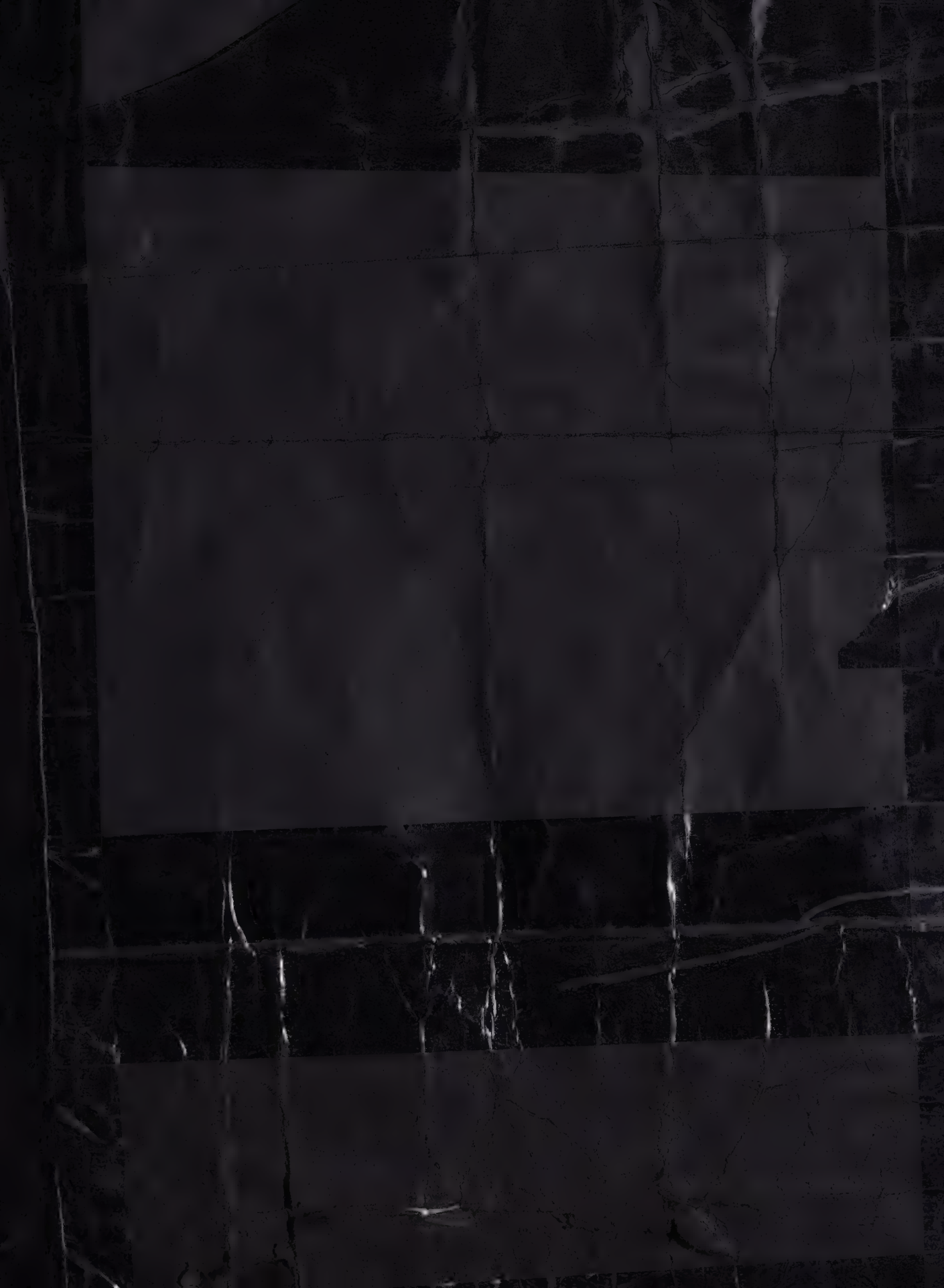
Auxiliary Power Supply Printed Board

AUX. POWER SUPPLY 1425

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1201	100k	CF			21819
CAPACITORS					
C1201	10000µF	E		16V	453459
C1202	10nF	CE(3)		25V	450548
C1203	2.2µF	T		35V	35930
C1204	2200µF	E		25/35V	454043
C1205	10nF	CE(3)		25V	450548
C1206	2.2µF	T		35V	35930
C1207	3300µF	E		16V	44512
C1208	10nF	CE(3)		25V	450548
C1209	2.2µF	T		35V	35930
C1210	100µF	MF		100V	37018
DIODES					
D1201		IN4003			23462
D1202		IN4003			23462
D1203		IN4003			23462
D1204		IN4003			23462
D1205		IN4003			23462
D1206		IN4003			23462
D1207		IN4003			23462
D1208		IN4003			23462
D1209		IN4003			23462
D1210		IN4003			23462
D1211		IN4003			23462
D1212		IN4003			23462
INTEGRATED CIRCUITS					
U1201		Voltage Regul.		5V	36170
U1202		Voltage Regul.		12V	36170
U1203		Voltage Regul.		-5V	36170

RES.		R1201
CAPS.		C1201 C1204 C1207 C1210
MISC.	D1202 D1203 D1206 D1207 D1210 D1211	D1201 D1204 D1205 D1208 D1209 D1212





C1203 C1206 C1209	
U1201 U1202 U1203	

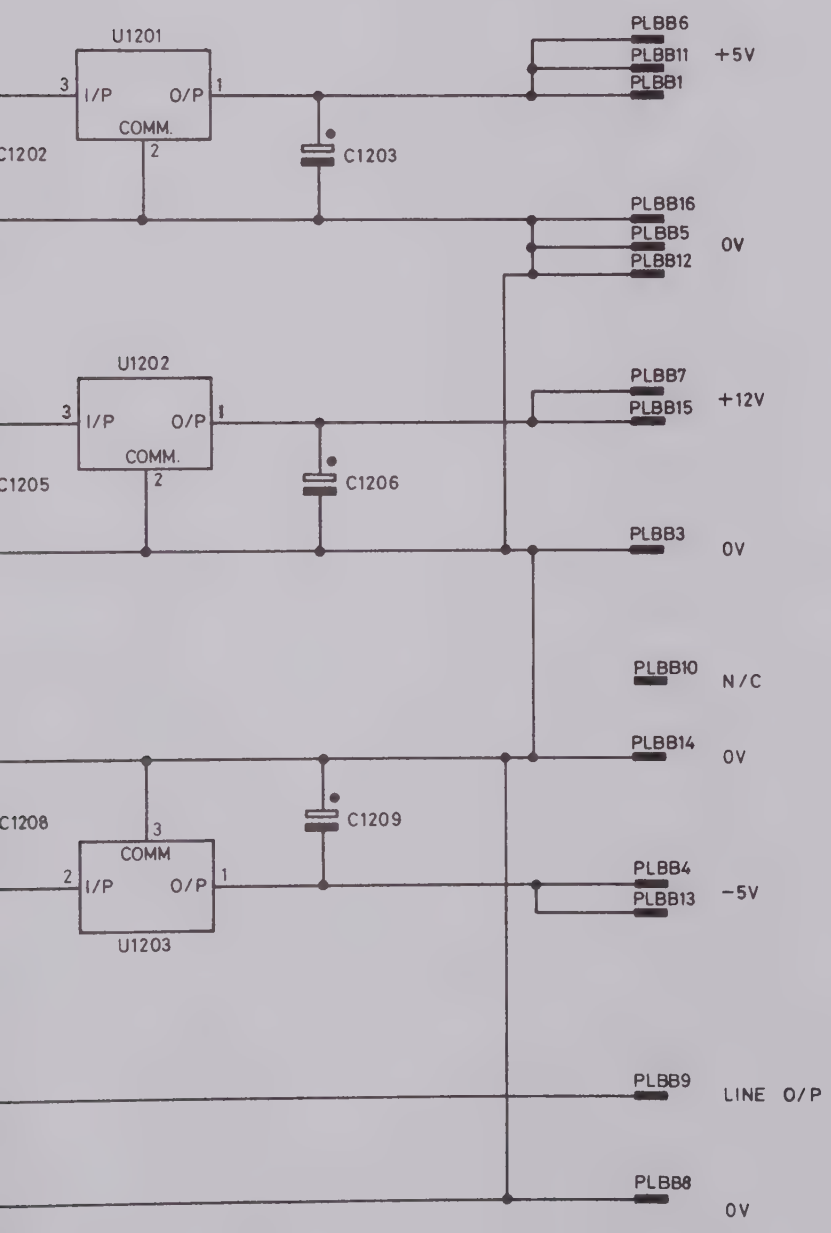
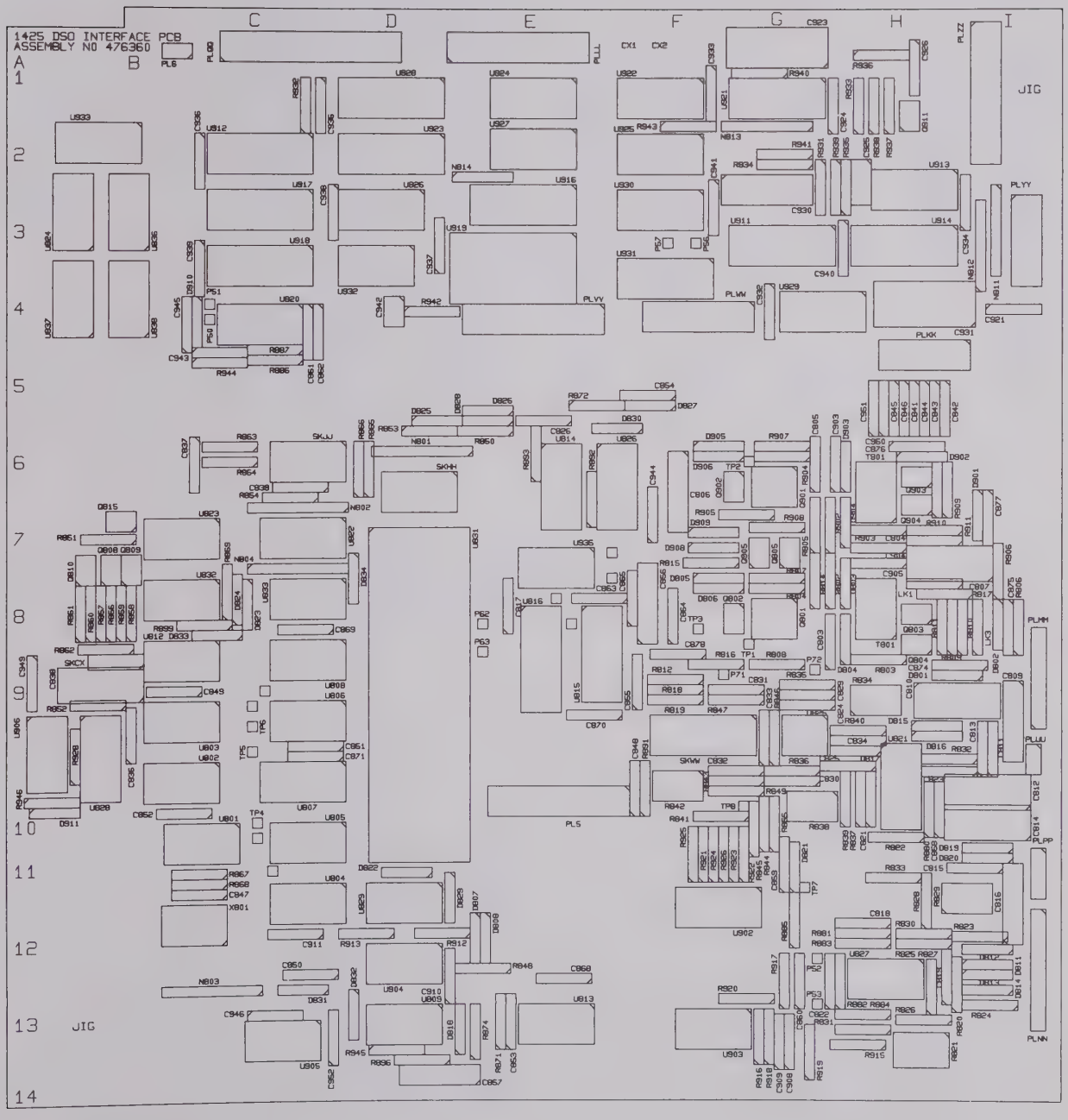


Fig. 12 Auxiliary Power Supply Circuit Diagram



Interface Printed Board

FOR COMPONENTS LIST SEE PAGES
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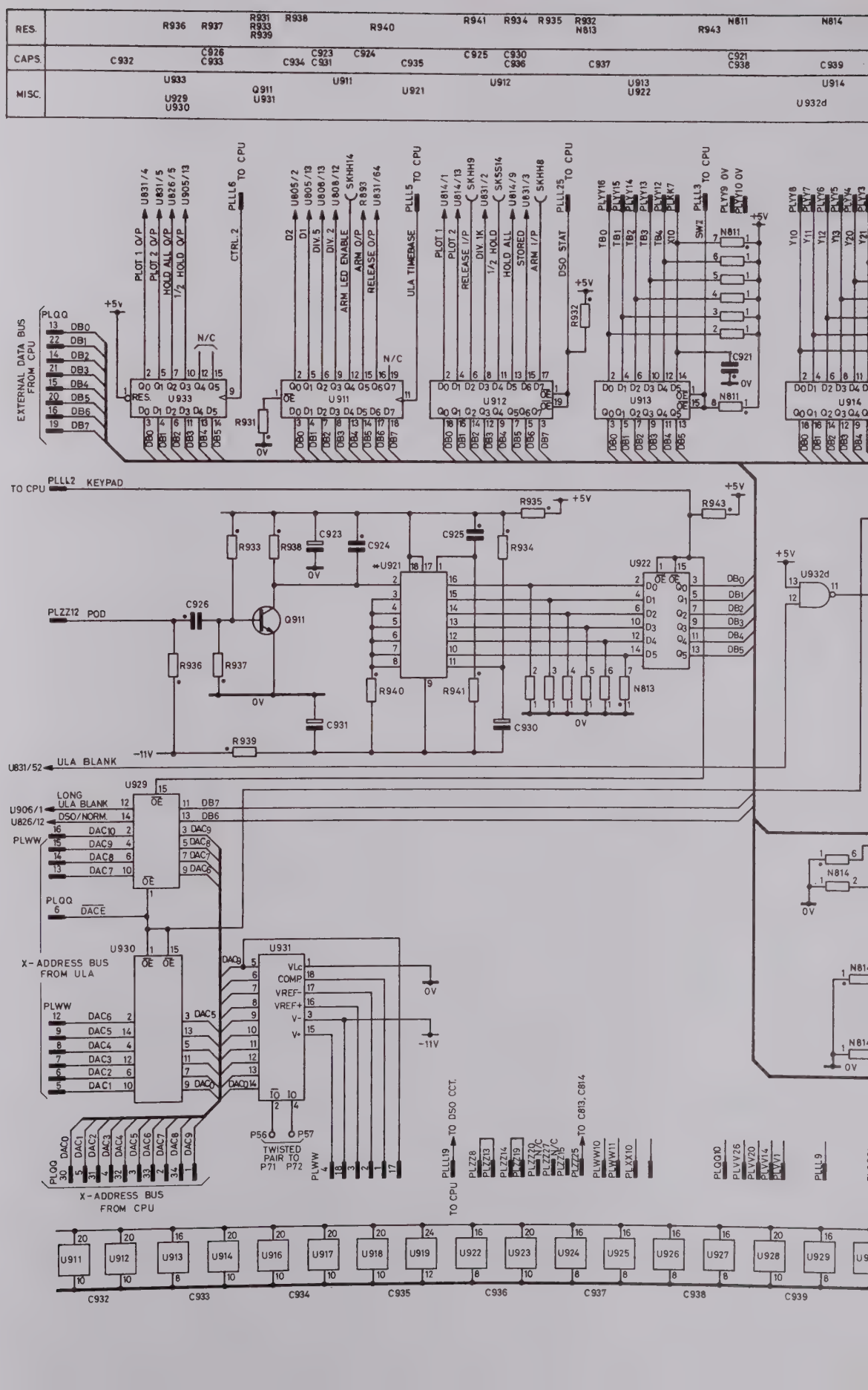
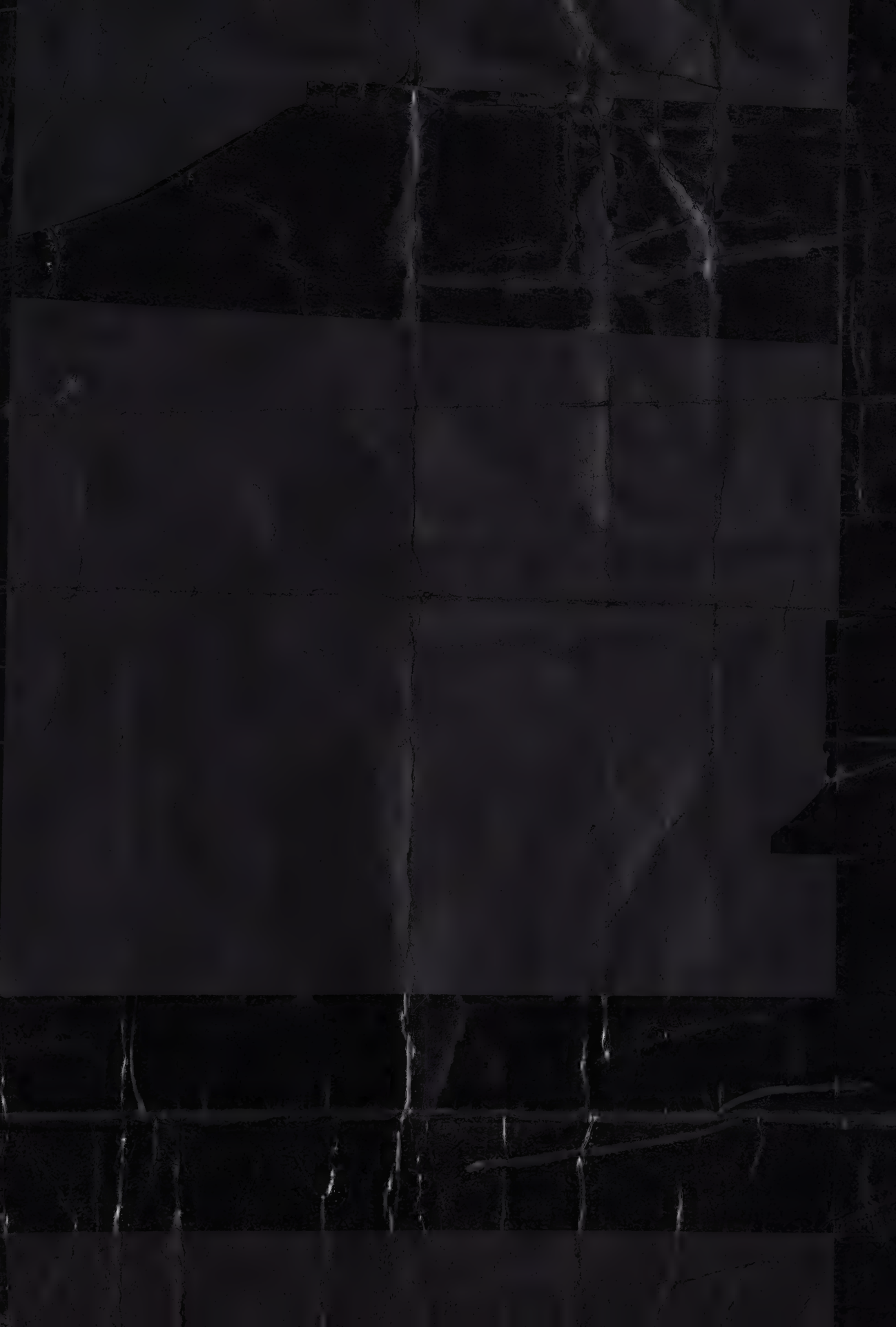

RES.
R936 R937 R931 R933 R939 R938 R940 R941 R934 R935 R932 N813 R943 N811 N814
CAPS.
C932 C926 C933 C934 C923 C931 C924 C935 C925 C930 C936 C937 C921 C938 C939
MISC.
U933 U929 U930 Q911 U931 U911 U921 U912 U913 U922 U914 U932d
EXTERNAL DATA BUS FROM CPU
PLQQ
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
+5v
PLOT 1 O/P
PLOT 2 O/P
HOLD ALL O/P
1/2 HOLD O/P
U831/4
U831/5
U826/5
U905/13
N/C
U933
RES.
PLLL6 TO CPU
CTRL 2
R931
0V
D2
D1
DIV 5
DIV 2
ARM LED ENABLE
ARM O/P
RELEASE O/P
U805/2
U805/13
U808/13
U808/12
SKHH14
R893
U831/64
U911
ULA TIMEBASE
PLLL5 TO CPU
PLOT 1
PLOT 2
RELEASE I/P
DIV 1K
1/2 HOLD
HOLD ALL
STORED
ARM I/P
U814/1
U814/13
U831/2
SKHH9
SKSS14
U814/9
U831/3
SKHH8
U912
DSO STAT
PLLL25 TO CPU
R932
PLYY16
PLYY15
PLYY14
PLYY13
PLYY12
PLYK7
TB0
TB1
TB2
TB3
TB4
X10
SW1
PLLL3 TO CPU
PLYY9 0V
PLYY10 0V
U913
C921
N811
Y10
Y11
Y12
Y13
Y20
Y21
U914
TO CPU PLLL2 KEYPAD
R933
R938
C923
C924
C925
R934
R935
R943
U921
U922
U932d
PLZZ12 POD
C926
Q911
R936
R937
R940
R941
C931
C930
N813
R939
-11V
U831/52 ULA BLANK
U929
LONG ULA BLANK
U906/1
DSO/NORM.
U826/12
PLWW
DAC10
DAC9
DAC8
DAC7
DB7
DB6
DAC9
DAC8
DAC7
DAC6
PLQQ
DACE
N814
U930
X-ADDRESS BUS FROM ULA
U931
DAC5
DAC6
DAC4
DAC3
DAC2
DAC1
DAC0
VLC
COMP
VREF-
VREF+
V-
V+
P56
P57
TWISTED PAIR TO P71 P72
X-ADDRESS BUS FROM CPU
PLLL19 TO DSO CCT.
TO CPU
PLZZ28
PLZZ13
PLZZ14
PLZZ19
PLZZ18
PLZZ17/C
PLZZ15
PLZZ25
TO C813, C814
PLWW10
PLWW11
PLXX10
PLQQ0
PLVV26
PLVV20
PLVV14
PLVV1
PLLL9
U911
U912
U913
U914
U916
U917
U918
U919
U922
U923
U924
U925
U926
U927
U928
U929
C932
C933
C934
C935
C936
C937
C938
C939



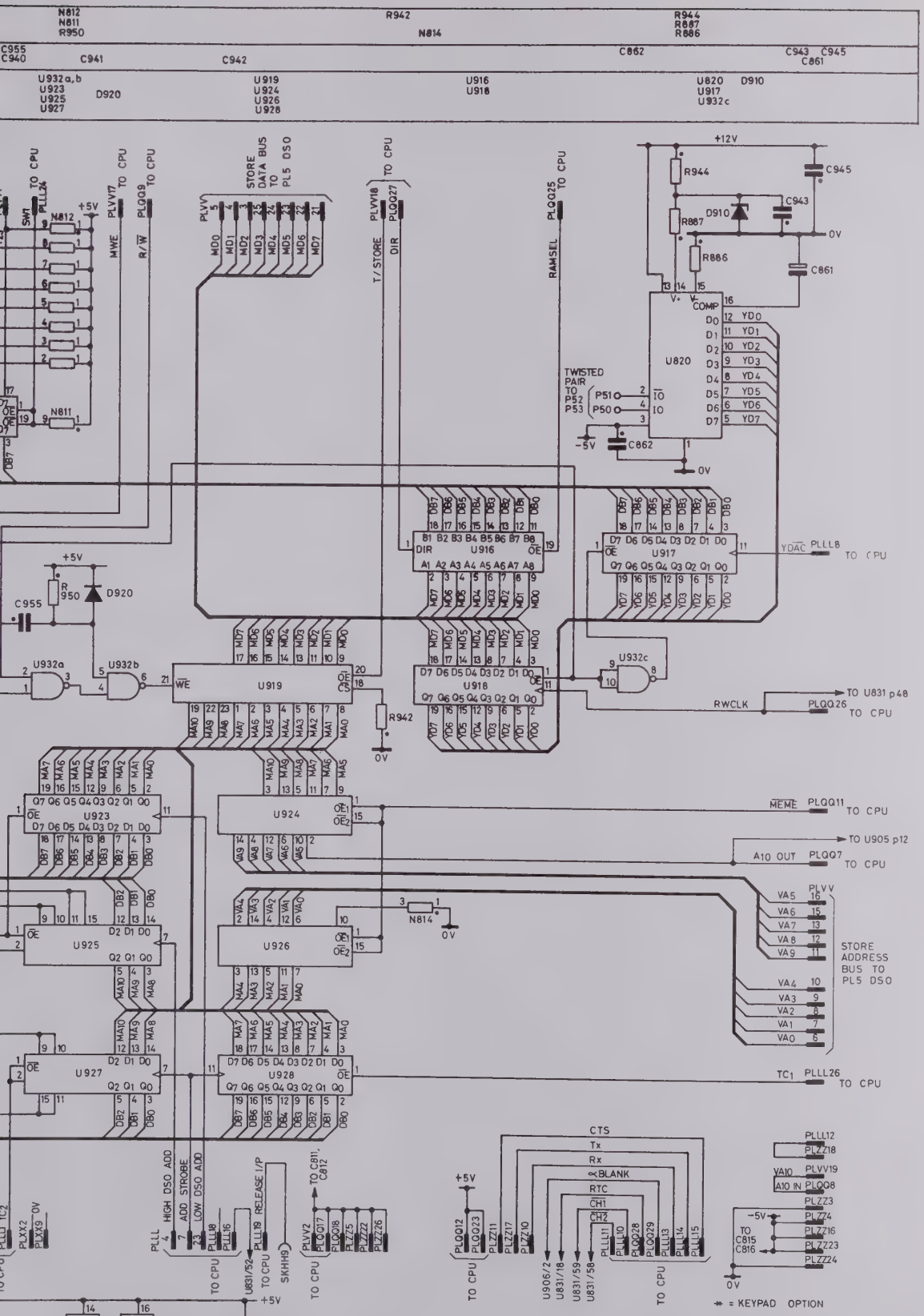
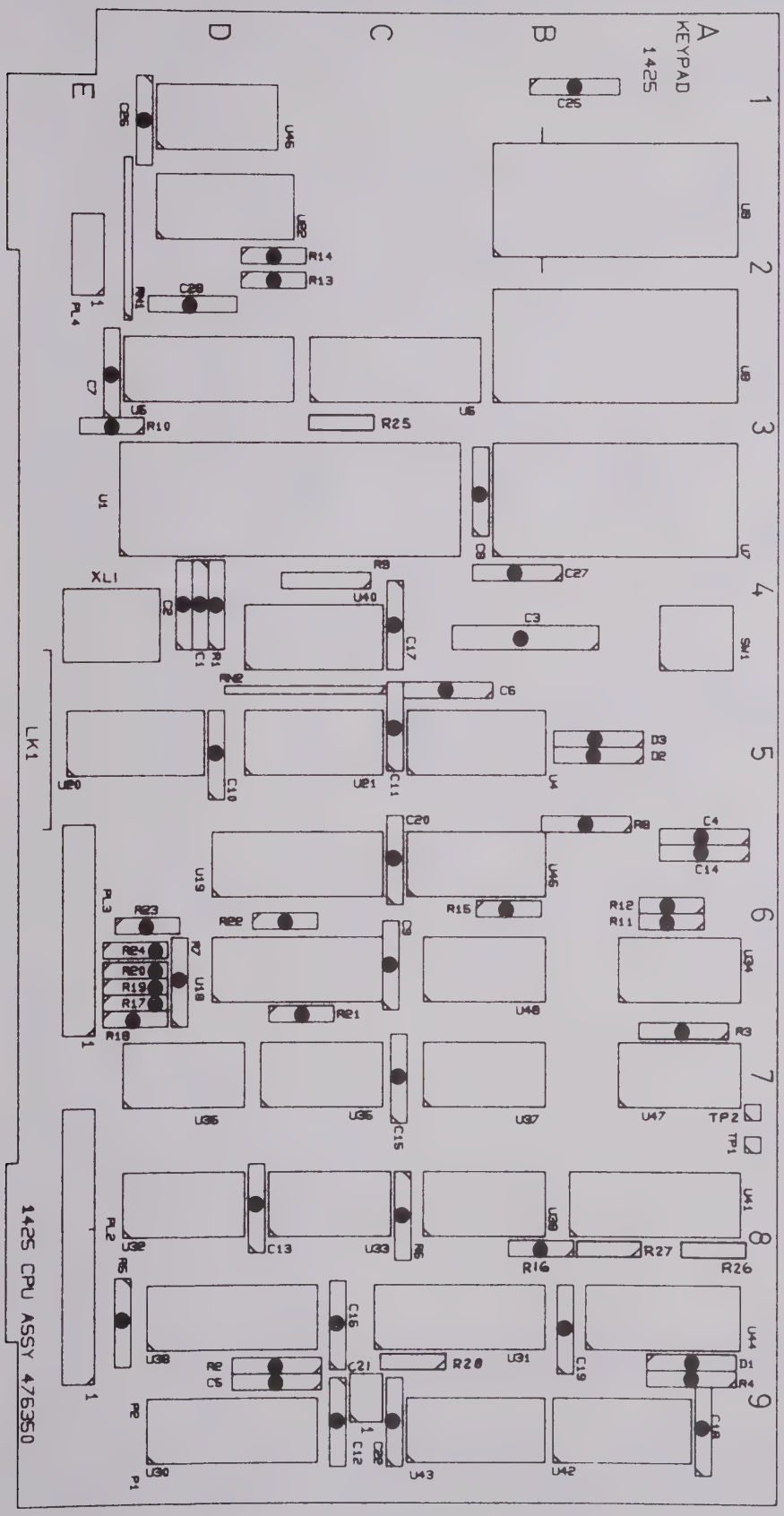


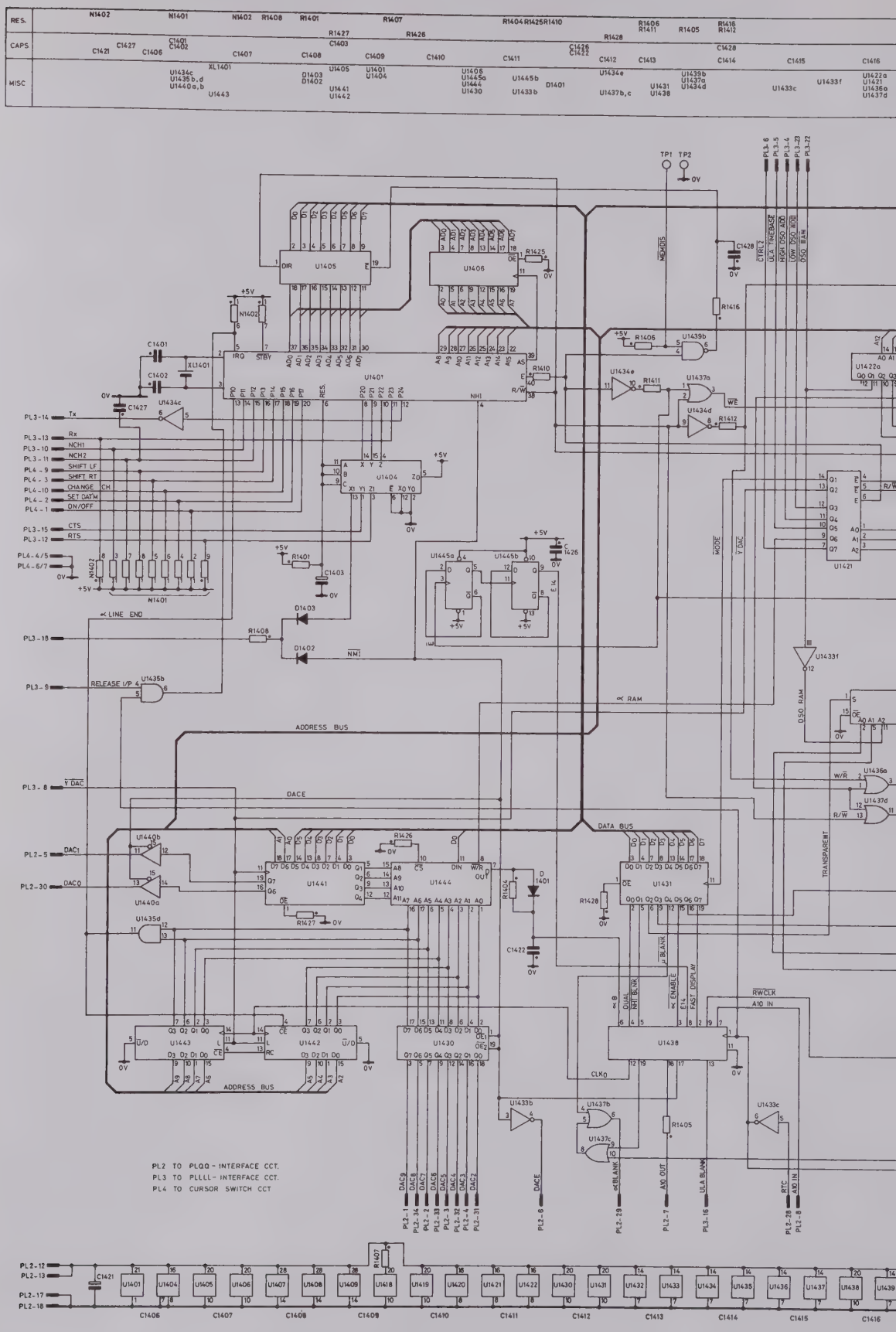
Fig. 13 Interface Circuit Diagram



C.P.U. Printed Board

CPU 1425

Ref	Value	Description	Tol %±	Rating	Part No	
RESISTORS						
C3	R1401	100k	CF		21819	
C8	R1402	10k	CF		21809	
A6	R1403	1k	CF		21799	
A8	R1404	220	CF		21796	
D8	R1405	100	CF		21794	
B7	R1406	47k	CF		21815	
C6	R1407	68	CF		28716	
A5	R1408	15k	CF		28727	
D2	R1410	180	CF	1/8W	43715	
A5	R1411	180	CF	1/8W	43715	
A5	R1412	180	CF	1/8W	43715	
C1	R1413	180	CF	1/8W	43715	
C1	R1414	180	CF	1/8W	43715	
A5	R1415	330	CF	1/8W	44220	
A7	R1416	180	CF	1/8W	43715	
D6	R1417	470	CF	1/8W	44222	
D6	R1418	470	CF	1/8W	44222	
D6	R1419	470	CF	1/8W	44222	
D5	R1420	470	CF	1/8W	44222	
C6	R1421	470	CF	1/8W	44222	
C5	R1422	470	CF	1/8W	44222	
D5	R1423	470	CF	1/8W	44222	
D5	R1424	470	CF	1/8W	44222	
	R1425	4k7	CF		21805	
	R1426	4k7	CF		21805	
	R1427	4k7	CF		21805	
	R1428	4k7	CF		21805	
	N1401	47kx8	Resistor Network		450602	
	N1402	47kx8	Resistor Network		450602	
CAPACITORS						
C3	C1401	15pF	CE(3)		42410	
C3	C1402	15pF	CE(3)		42410	
A3	C1403	10µF	E	25V	32180	
A5	C1404	100pF	CE(3)		42420	
C8	C1405	100pF	CE(3)		42420	
B4	C1406	10nF	CE(3)	25V	450548	
D2	C1407	10nF	CE(3)	25V	450548	
A3	C1408	10nF	CE(3)	25V	450548	
B6	C1409	10nF	CE(3)	25V	450548	
C4	C1410	10nF	CE(3)	25V	450548	
B4	C1411	10nF	CE(3)	25V	450548	
B8	C1412	10nF	CE(3)	25V	450548	
C7	C1413	10nF	CE(3)	25V	450548	
A5	C1414	10nF	CE(3)	25V	450548	
B6	C1415	10nF	CE(3)	25V	450548	
B8	C1416	10nF	CE(3)	25V	450548	
B4	C1417	10nF	CE(3)	25V	450548	
A8	C1418	10nF	CE(3)	25V	450548	
A8	C1419	10nF	CE(3)	25V	450548	
B5	C1420	10nF	CE(3)	25V	450548	
B8	C1421	22µF	T	35V	35932	
B8	C1422	3.3nF	CE(3)	50V	42438	
C1425	100nF	CE(3)		50V	43498	A1
C1426	100nF	CE(3)		50V	43498	C1
C1427	100nF	CE(3)		50V	43498	A3
C1428	56pF	CE(3)		50V	42417	C1
DIODES						
D1401		IN4148			23802	A3
D1402		IN4148			23802	A4
D1403		IN4148			23802	A4
INTEGRATED CIRCUITS						
U1401		HD63A03			453655	C3
U1404		4053			41891	B4
U1405		74ALS245			451953	C2
U1406		74HC373			452559	B1
U1407		Programmed			480061	A3
U1408		Not Fitted				
U1409		MB8128-15 or MBM8128-15			450683	A3
U1418		74HC373			452559	C6
U1419		74HC373			452559	C5
U1420		74HC138			452561	D4
U1421		74HC138			452561	C4
U1422		74HC139			452562	C1
U1430		74C244			450913	C3
U1431		74C374			451266	B8
U1432		74HC164			452563	C7
U1433		74HC04			451958	C7
U1434		74HC04			451958	A6
U1435		74HC08			451959	C6
U1436		74HC32			452265	C6
U1437		74HC32			452265	B6
U1438		Pal. 16R4 PROG.			480051	C8
U1439		74HC00			451956	B7
U1440		4503			41295	C4
U1441		74C374			451266	A7
U1442		74LS191			41092	A8
U1443		74LS191			41092	B8
U1444		HM6147-85			452621	A8
U1445		74C74			451290	C1
U1446		74HC157			451964	B5
U1447		74HC32			452265	A6
U1448		74HC08			451959	B6
SWITCHES						
S1401		Dil 4-Bank S/P			453785	A4
MISCELLANEOUS						
XL1401		Crystal 4.9152MHz			453661	
PL2					453727	D8
PL3					453745	D6


RES-
CAPS
MISC
N1402
N1401
R1408
R1401
R1407
R1404 R1425 R1410
R1406 R1411
R1405
R1416 R1412
R1427
R1426
C1403
R1428
C1426 C1422
C1428
C1421
C1427
C1406
C1401 C1402
C1407
C1408
C1409
C1410
C1411
C1412
C1413
C1414
C1415
C1416
XL1401
U1434c U1435b,d U1440a,b
U1443
D1403 D1402
U1405
U1401 U1404
U1441 U1442
U1406 U1445a U1444 U1430
U1445b
D1401
U1433b
U1434e
U1437b,c
U1431 U1438
U1439b U1437a U1434d
U1433c
U1433f
U1422a U1421 U1436a U1437d
TP1 TP2
0V
PL3-6
PL3-5
PL3-4
PL3-3
PL3-2
PL3-1
MEMDIS
CTRL2
ULA TIMEBASE
HIGH DS50 ADD
LOW DS50 ADD
DS50 RAM
U1405 DIR
U1406
R1425
R1416
C1428
+5V
N1402
C1401
C1402
XL1401
U1401
IRQ
STBY
R1410
R1406
U1439b
U1434e
R1411
U1437a
U1434d
R1412
WE
R/W
NMI
C1427
U1434c
PL3-14 Tx
PL3-13 Rx
PL3-10 NCH1
PL3-11 NCH2
PL4-9 SHIFT LF
PL4-3 SHIFT RT
PL4-10 CHANGE CH
PL4-2 SET DATM
PL4-1 ON/OFF
PL3-15 CTS
PL3-12 RTS
U1404
R1401
C1403
N1402
N1401
PL4-4/5
PL4-6/7
D1403
D1402
R1408
PL3-18
PL3-9
RELEASE I/P
U1435b
U1445a
U1445b
C1426
MODE
V DAC
U1421
U1433f
U1436a
U1437d
DS50 RAM
TRANSPARENT
LINE END
RAM
ADDRESS BUS
DATA BUS
DACE
PL3-8
V DAC
PL2-5 DAC1
PL2-30 DAC0
U1440b
U1440a
U1435d
R1426
R1427
U1441
U1444
R1404
D1401
R1428
U1431
C1422
BLANK
ENABLE
FAST DISPLAY
DUAL
NRT BLNK
RWCLK
A10 IN
U1438
CLK0
U1443
U1442
U1430
U/D
ADDRESS BUS
U1433b
U1437b
U1437c
R1405
U1433c
PL2 TO PLQQ - INTERFACE CCT.
PL3 TO PLLLL - INTERFACE CCT.
PL4 TO CURSOR SWITCH CCT
DAC9
DAC8
DAC7
DAC6
DAC5
DAC4
DAC3
DAC2
DACE
BLANK
A10 OUT
ULA BLANK
RTC
A10 IN
PL2-1
PL2-34
PL2-2
PL2-33
PL2-3
PL2-32
PL2-4
PL2-31
PL2-6
PL2-29
PL2-7
PL3-16
PL2-28
PL2-8
PL2-12
PL2-13
PL2-17
PL2-18
C1421
R1407
U1401
U1404
U1405
U1406
U1407
U1408
U1409
U1418
U1419
U1420
U1421
U1422
U1430
U1431
U1432
U1433
U1434
U1435
U1436
U1437
U1438
C1406
C1407
C1408
C1409
C1410
C1411
C1412
C1413
C1414
C1415
C1416

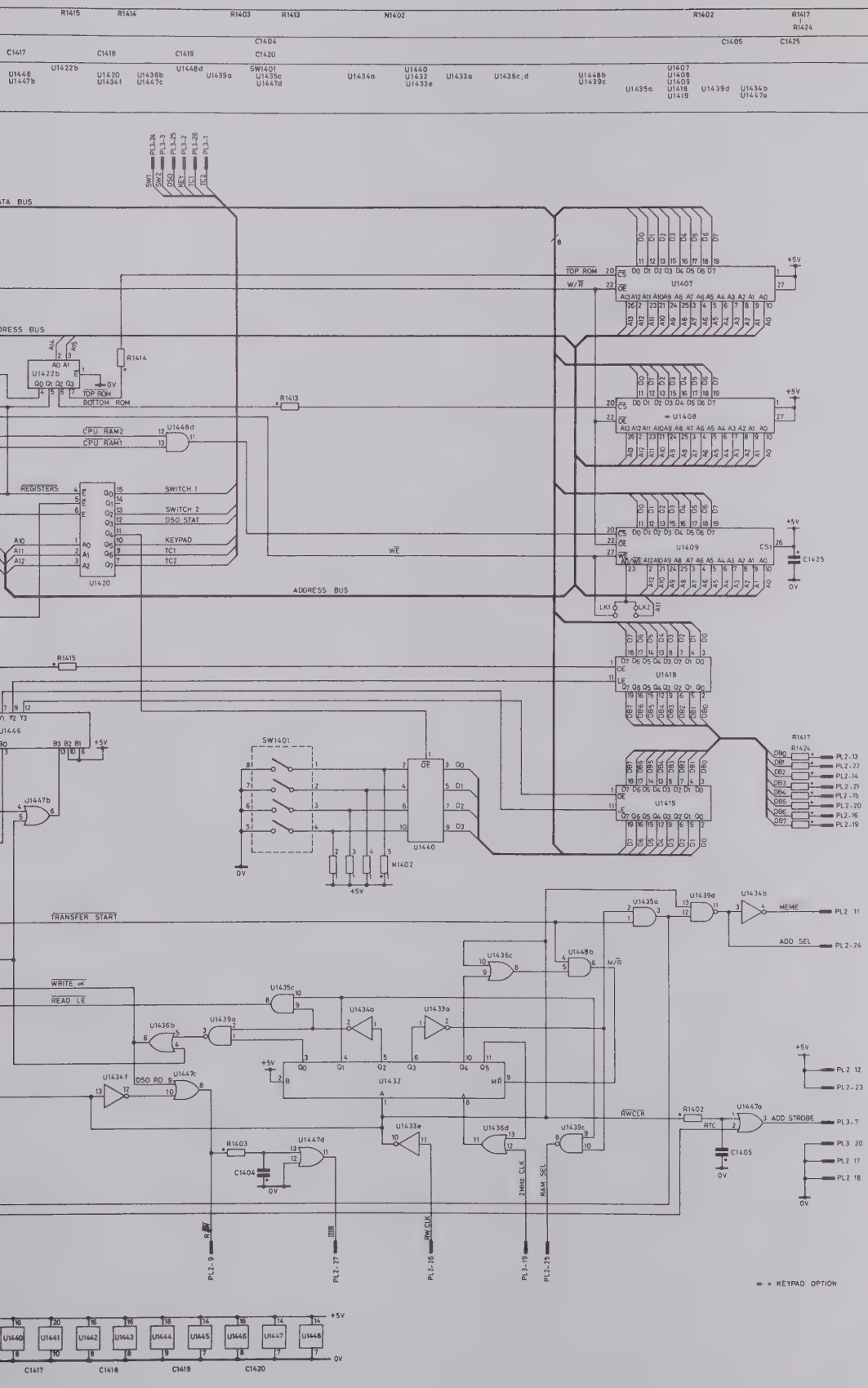
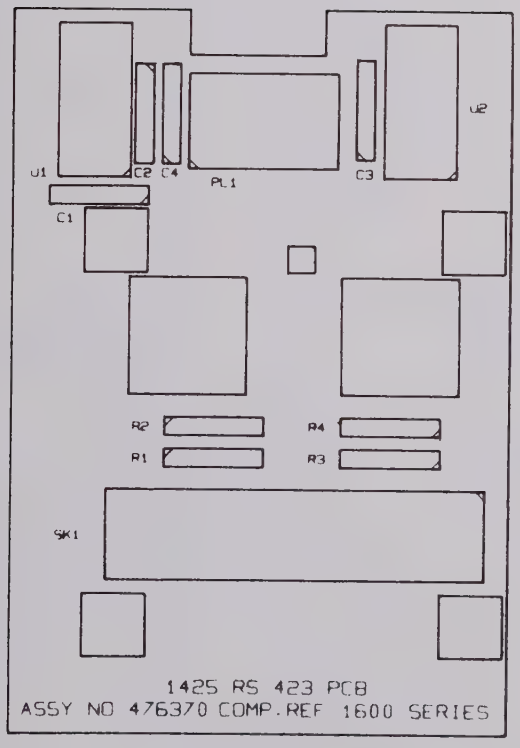


Fig. 14 CPU Board Circuit Diagram



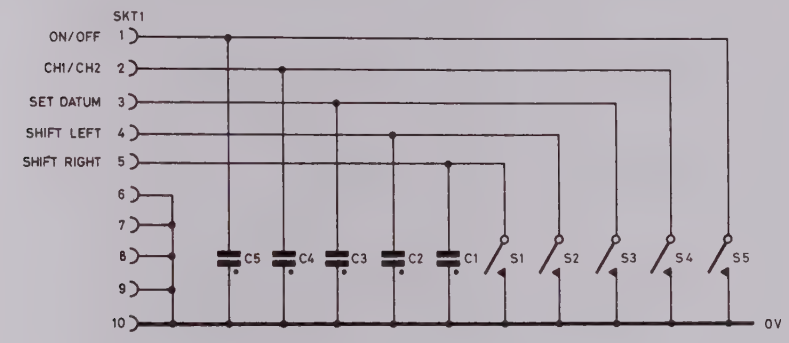
RS423 Printed Board

CURSOR, SWITCH PICKOFF & RS423 1425

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS					
C1	10nF	CE(3)		25V	450548
C2	10nF	CE(3)		25V	450548
C3	10nF	CE(3)		25V	450548
C4	10nF	CE(3)		25V	450548
C5	10nF	CE(3)		25V	450548
SWITCHES					
S1		Switch Tact			453744
S2		Switch Tact			453744
S3		Switch Tact			453744
S4		Switch Tact			453744
S5		Switch Tact			453744
RESISTORS					
R1601	3k3	CF			21803
R1602	3k3	CF			21803
R1603	4k7	CF			21805
R1604	4k7	CF			21805
CAPACITORS					
C1601	47pF	CE(3)			42416
C1602	47pF	CE(3)			42416
C1603	10nF	CE(3)		25V	450548
C1604	10nF	CE(3)		25V	450548

Ref	Value	Description	Tol %±	Rating	Part No
INTEGRATED CIRCUITS					
U1601		AM26LS29			453501
U1602		AM26LS32			453502
SOCKETS					
SK1601		25-way 'D' type			453367
CAPACITORS					
C1701	10nF	CE(3)		25V	450548
C1702	10nF	CE(3)		25V	450548
C1703	10nF	CE(3)		25V	450548
C1704	10nF	CE(3)		25V	450548
C1705	10nF	CE(3)		25V	450548
C1706	10nF	CE(3)		25V	450548
C1707	10nF	CE(3)		25V	450548
C1708	10nF	CE(3)		25V	450548
C1709	10nF	CE(3)		25V	450548
C1710	10nF	CE(3)		25V	450548
C1711	10nF	CE(3)		25V	450548
C1712	10nF	CE(3)		25V	450548
C1713	10nF	CE(3)		25V	450548
SWITCHES					
S1					453673
S2					453673
S3					453673
SOCKETS					
SK1701		16-way Cable			453882

RES.		R1601 R1602 R1603
CAPS.	C5 C4 C3 C2 C1	C1604 C1602 C1601
MISC.	S1 S2 S3 S4 S5 U1601	PL1601 SK1601



WAFERS VIEWED FROM FRONT OF 'SCOPE.

ATTENUATOR SET TO 10V / DIV.

TIMEBASE SET TO 0·2 secs / DIV

Fig. 15 Cursor Switch Board Circuit Diagram

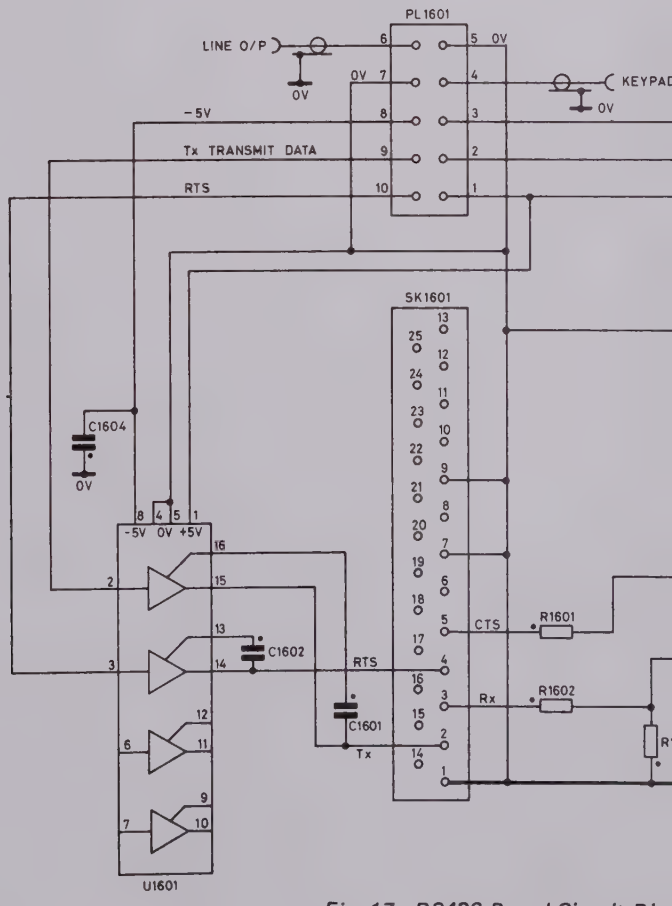
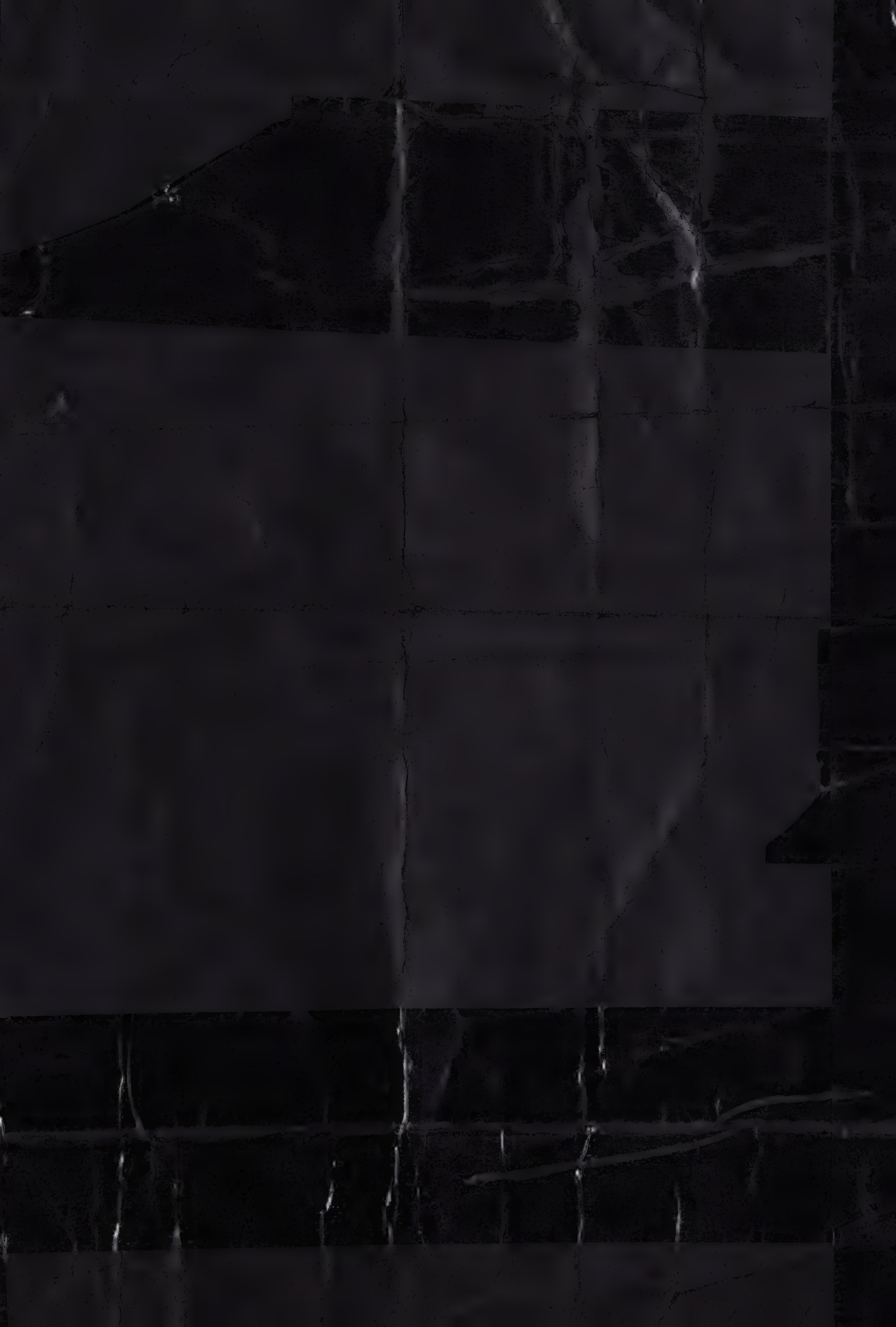
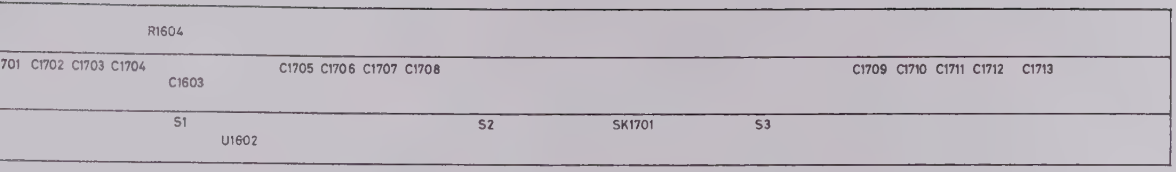


Fig. 17 RS423 Board Circuit Diag





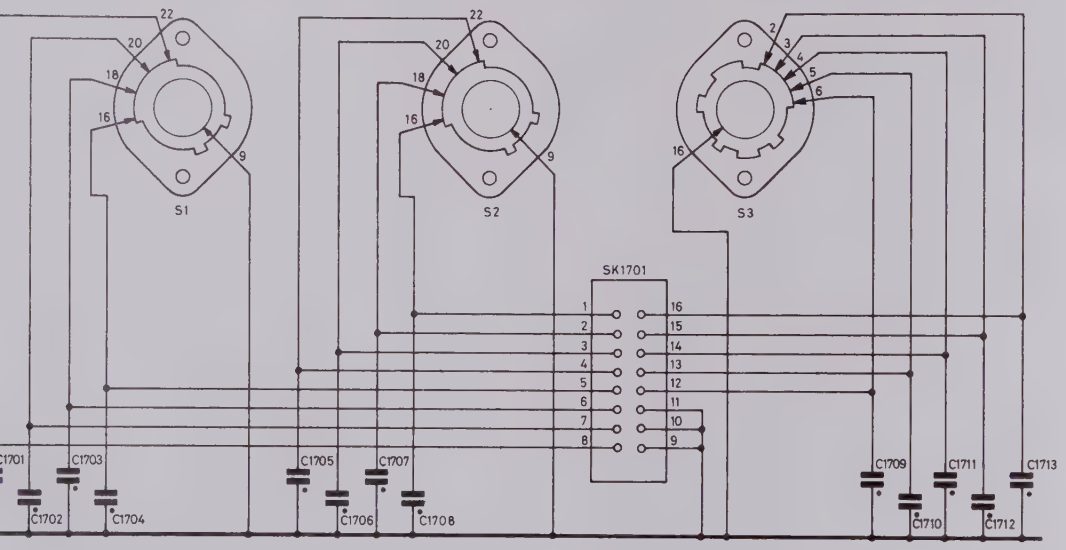


Fig. 16 Switch Pick-Off Circuit Diagram

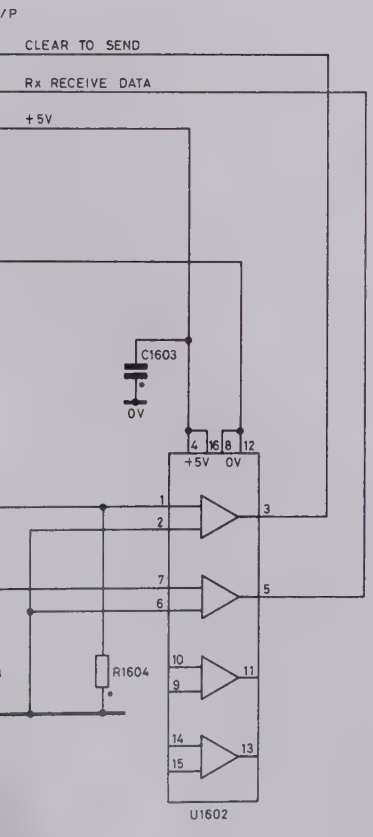
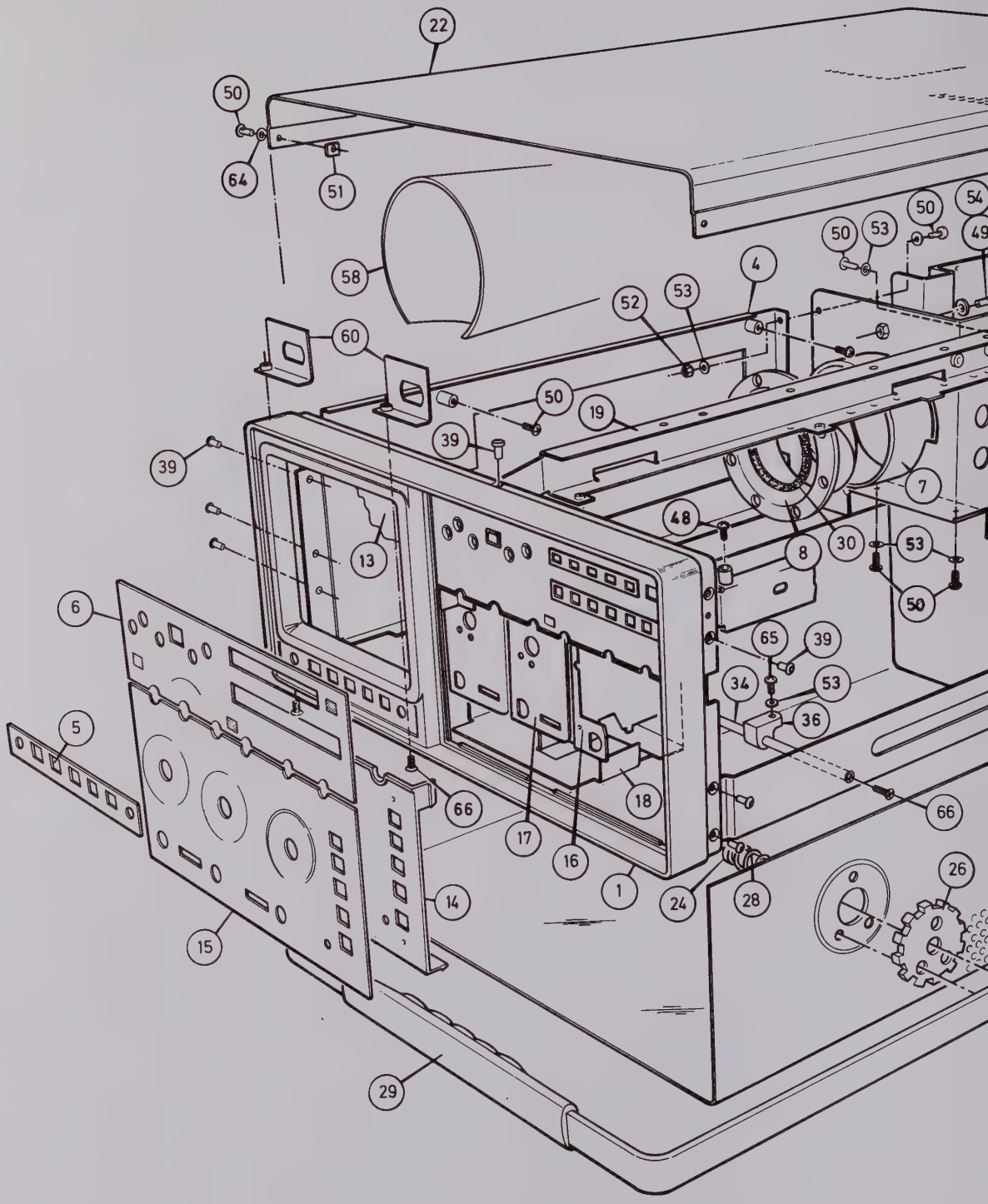


Fig. 15 *Fig. 16* *Fig. 17*

Cursor Switch Board, Switch Pick-Off, RS423 Board Circuit Diagram

1425 MECHANICAL PARTS LIST

Ref. No.	Part No.	Description	Units
1	453600	Frame/Panel	
2	453844	Panel Read	
3	450730	Support Side (Long)	
4	453489	Side Panel LH	
5	453599	Coverlay Cursor	
6	454067	Coverlay Pushbuttons	
7	453613	Base C.R.T. Moulding	
8	453614	Clamp C.R.T. Moulding	
9	453636	Cover Rear Moulding	
10	40068	Fuse Holder	
11	44960	Connector Supply	
12	453488	Side Plate RH	
13	453770	Filter Grey	
14	452915	Panel Front	
15	454071	Coverlay	
16	453616	Screen Timebase	
17	453617	Screen Attenuator	
18	453457	Screen BNC Sockets	
19	450648	Heatsink	
20	454044	Heatsink (Aux. Power Supply)	
21	453169	Case Bottom	
22	453167	Case Top	
23	36681	Button Handle	
24	44470	Spindle Moulded	
25	452906	Cover Handle	
26	452905	Base Handle	
27	452901	Foot	
28	44568	Spring	
29	452217	Handle Assy.	
30	44963	Washer C.R.T.	
31	453432	Knob Pushbutton	
32	453434	Knob 10mm 'D' Type	
33	453445	Knob 15mm	
34	453490	Bar Support	
35	453440	Knob 21mm	
36	39873	Hinge	
37	453444	Cap 21mm	
38	453443	Cap 15mm	
39	450690	POP Rivet	
40	12862	Rivet	
41	29426	Rivet	
42	453431	Bezel	
43	382	Grommet	
44	24159	Terminal	
45	33685	Fuse 500mA	
46	33684	Fuse 250mA	
47	33077	Screw M4 x 12 C'sk. Hd.	
48	33032	Screw M2.5 x 6 Pan Hd.	
49	33045	Screw M4 x 10 Pan Hd.	
50	33038	Screw M3 x 8 Pan Hd.	
51	41407	Nut M3 Square	
52	33023	Nut M3	
53	33016	Washer Wavey	
54	33017	Washer M4 Wavey	
55	453740	Label	
56	453487	Keytop	
57	453503	Mounting Plate	
58	453573	Shield C.R.T.	
59			
60	453491	Bracket Pot Mtg.	
61	453436	Knob 10mm x 4mm	
62	453442	Cap 10mm	
63	33037	Screw M3 x 6 Pan Hd.	
64	33003	Washer M3 Plain	
65	450460	Screw No.4 x 3/8" Type B	
66	33069	Screw M3 x 8 C'sk.	


22
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64
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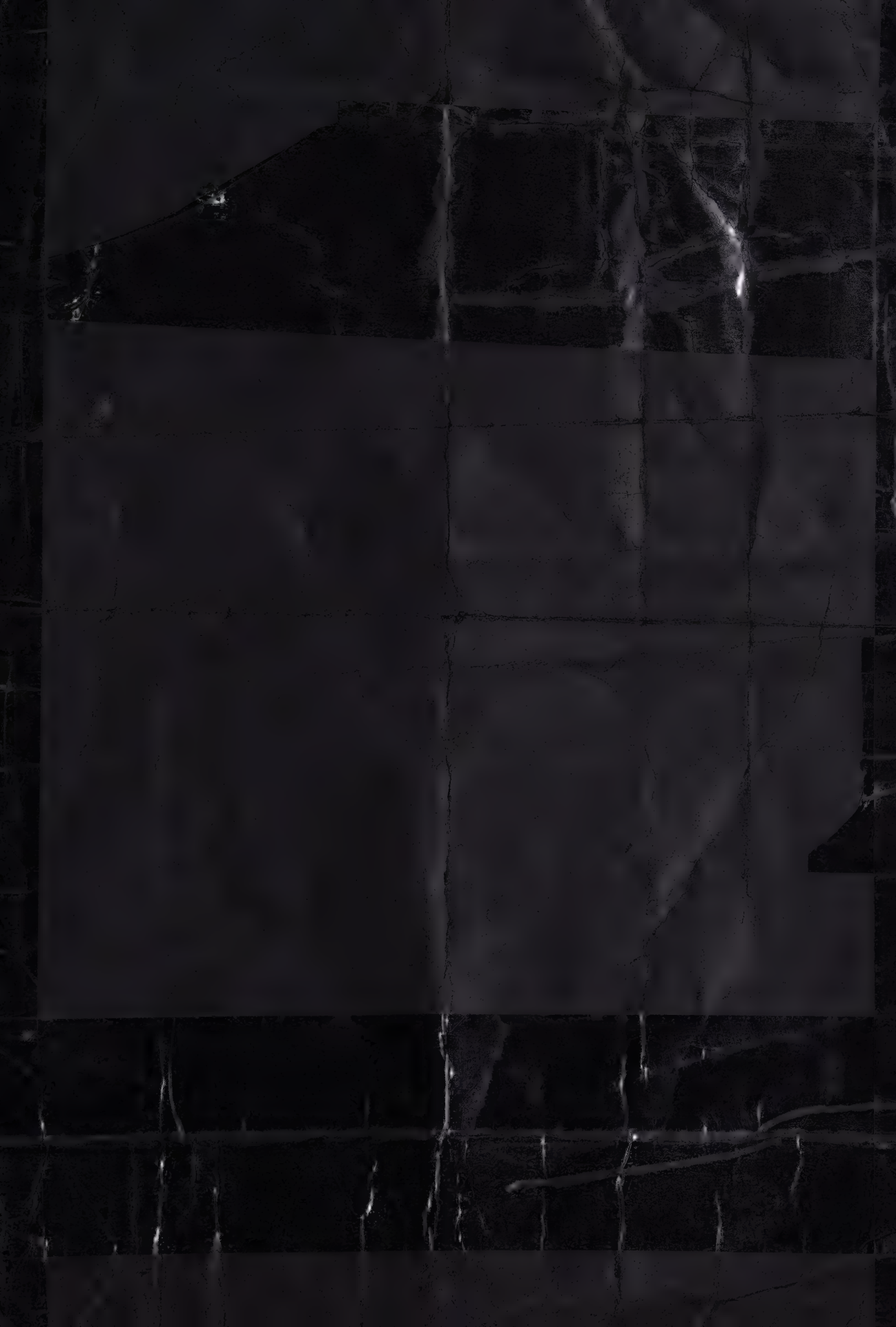

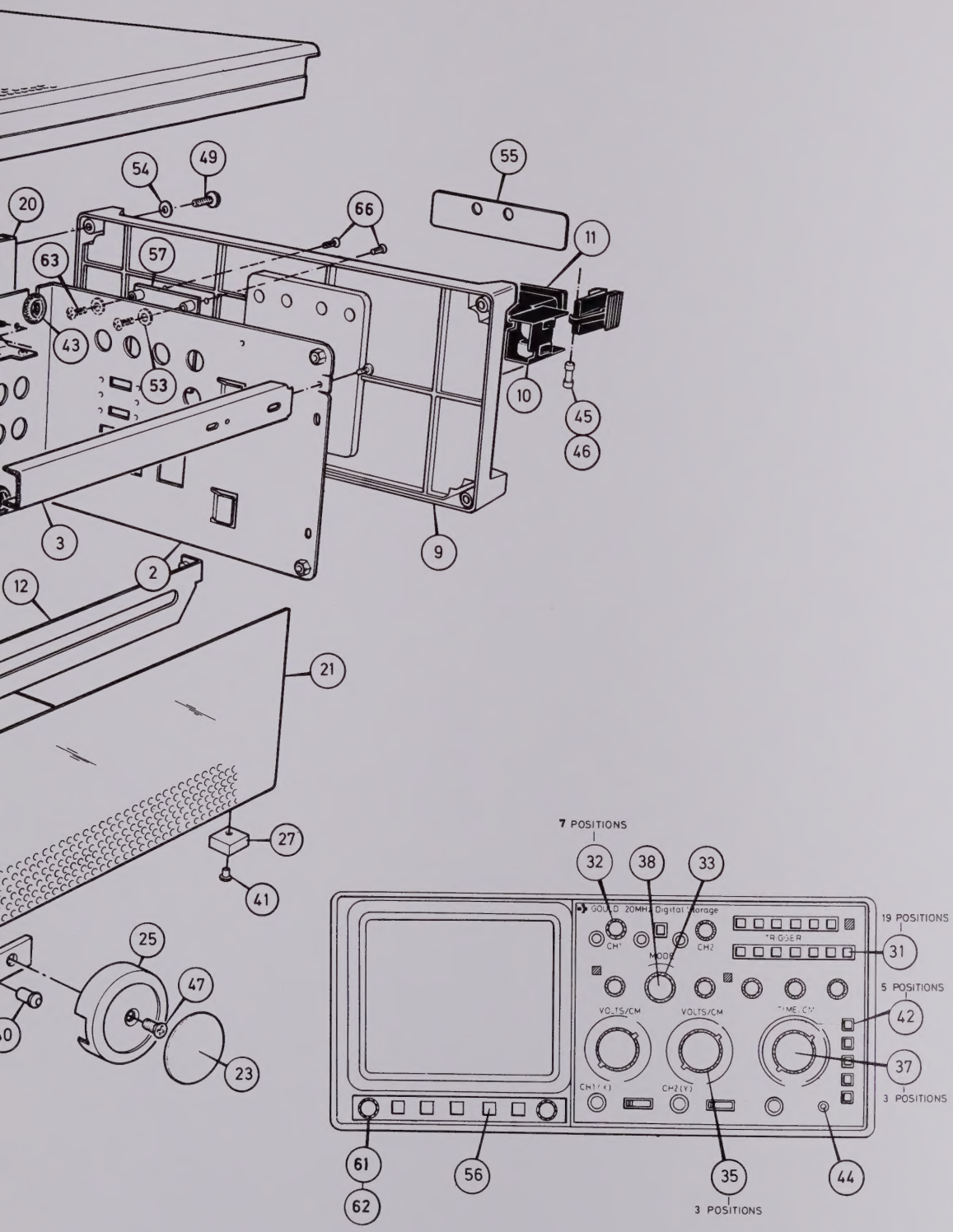

Fig. 18 Mechanical View

Guarantee and Service Facilities

Section 7

This instrument is guaranteed for a period of two years from its delivery to the purchaser, covering faulty workmanship and replacement of defective parts other than cathode ray tubes and batteries (where fitted). Cathode ray tubes are subject to the manufacturers guarantee. This assumes fair wear and tear and usage in the specified environment and does not cover routine recalibrations and mechanical adjustments.

We maintain comprehensive after sales facilities and the instrument should be returned to our factory for servicing if this is necessary. The type and serial number of the instrument should always be quoted, together with full details of any fault and service required.

Equipment returned for servicing must be adequately packed, preferably in the box in which the instrument was supplied and shipped with transportation charges prepaid. We accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired the repair will be put in hand without delay and charged unless other instructions are received.

Our Sales, Service and Engineering Departments are ready to assist you at all times.

The Service Department can provide maintenance and repair information by telephone or letter, if required.

Note: Please check fuses before returning instruments for service and ensure that any 13 Amp mains plugs fitted are removed. To prevent possible transit damage, we regret that mains plugs cannot be returned.

Service Dept.,
Roebuck Road,
Hainault,
Essex,
IG6 3UE

Tel: 01-500 1000
Telex: 263785
Telegrams: Attenuate Ilford

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